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To this end, we have carried out a comprehensive detailed modeling of electronic post-optical detection amplifiers based on CMOS technology. We have optimized such receivers for FSOI applications. We have validated our models by experimental verification using MOSIS foundry. We have demonstrated the successful operation of CMOS trans-impedance amplifier based receivers favricated in 0.35 micron process with optimized performance for FSOI links performance.

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Final Technical Report

OPTICAL RECEIVER DEVELOPMENT FOR HIGH SPEED FREE-SPACE OPTICAL INTERCONNECTS

Ultra Program

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1. Objectives and Accomplishments

1.1. Objectives

The main objective of this program was the development of innovative optical receiver technologies that may satisfy the requirements imposed by free-space optical interconnects. Our proposed approach included:

i) Evaluation of technologies that enable the amplification of signals optically prior to photodetection or electrically afterwards.
ii) Development and characterization of novel optical-amplifier technologies that could provide potentially low power, small physical size, large bandwidth, and integrability with Si-CMOS technology.
iii) Study of the integration of amplifiers with silicon IC's by flip-chip bonding technology.

1.2. Accomplishments

With these broad objectives in mind the following studies underlined below have lead to the following accomplishments:

1.2.1. Modeling of electronic receiver circuits and investigation of the performance scaling of these receivers with the scaling of microfabrication technologies.

To this end, we have carried out a comprehensive detailed modeling of electronic post-optical detection amplifiers based on CMOS technology. We have optimized such receivers for FSOI applications. We have validated our models by experimental verification using MOSIS foundry. We have demonstrated the successful operation of CMOS trans-impedance amplifier based receivers fabricated in 0.35micron process with optimized performance for FSOI links performance. This work resulted in the following two journal publications:

D.A. Van Blerkom, Fan, C., Blume, M., and Esener, S.C., "Transimpedance receiver design optimization for smart pixel arrays," *Journal of Lightwave Technology*, vol.16, no.1, IEEE, p.119-26, January 1998.

Kibar, O.; Van Blerkom, D.A.; Fan, C.; Esener, S.C., "Power minimization and technology comparisons for digital free-space optoelectronic interconnections", Journal of Lightwave Technology, vol.17, (no.4), IEEE, p.546-55, April 1, 1999

and a Ph.D. thesis

D. A. Van Blerkom, " Mixed signal CMOS circuits for Free Space Optical Interconnects: Design, Optimization and System Integration", Ph.D. Thesis, UCSD, 2000

Details of this work is presented in Appendix III and IV. These sections are partial reprints of the Van Blerkom Ph. D. thesis.

1.2.2. Modeling and evaluation of optical pre-amplification techniques

1.2.2.1. Investigation of the applicability of doubly-resonant optical parametric amplifier to FSOI

We have evaluated the possibility of using optical parametric amplifiers in FSOI. We studied and modeled such amplifiers. However, we have concluded at the end of the first year that these types of amplifiers will remain too bulky for use in integrated FSOI systems. We have than focused our research effort onto VCSEL amplifiers.

1.2.2.2. Investigation of VCSEL amplifiers and optimization of the gain-bandwidth product and the optical coupling efficiency for FSOI applications.

To this end, we have designed, modeled and evaluated VCSEL amplifiers. We have investigated the trade-off between the threshold power and the optical gain. We have studied methods to improve the coupling efficiency of the optical signals to the VCSEL amplifier. Our findings are summarized in the following publication

Kibar, O., Van Blerkom, D., Fan, C., P. J. Marchand, P.J., and Esener, S.C., "Small Signal Equivalent Circuits for a Semiconductor Laser," *Applied Optics 37*, pp. 6136-6139, September 1998.

This investigation constituted the bulk of our research effort in this program and led to the conclusion that optical amplifier arrays based on the VCSEL structure are feasible. We believe that such optical amplifiers can find applications in different fields ranging from free space optical interconnects and communications (including satellite communication) to Lidar applications for 3-D imaging. A detailed summary of these results is provided below.

Details of this study is presented in Appendix V. These sections are partial reprints of the Van Blerkom Ph. D. thesis.

1.2.3. Experimental demonstration and characterization of a VCSEL amplifier

To this end we have experimentally characterized the relevant properties such as optical gain, signal bandwidth, and RIN noise of single element VCSEL amplifiers. We have also studied approaches to convert the VCSEL amplifier into a low voltage light modulator. Our studies led to the following publications

Kibar, O.; Marchand, P.J.; Esener, S.C., "Gain-bandwidth product of a VCSEL amplifier", Conference Proceedings. LEOS '98. 11th Annual Meeting, Orlando, FL, USA, Piscataway, NJ, USA: IEEE,. p.221-2 vol.2, Dec. 1998

Wen, P., Sanchez, M., Kibar, O., Esener, S.C., "Low-voltage, high contrast-ratio, low-noise VCSEL modulator," OSA topical meeting on Optical Amplifiers and Their Applications, Quebec City, Canada, July 1, 2000

A patent disclosure has been submitted on the low voltage modulator application.

Esener, S.C., Kibar, O., "Ultra-Low Voltage, High Contrast Ratio, High Speed Spatial Light Modulator" UC#1999-075

Details of these studies are presented in Appendix V

2. Background

Free-space optical interconnects (FSOI) are being considered as a potential technological approach for reducing the latency and the power dissipation of off-chip data communications. Compared to an all-electronic processing system, a free-space

optical interconnection system contains photonics layers that provide electrical-to-optical and optical-to-electrical signal conversions. Photonics layers typically include optical transmitters and their associated drivers in the input plane, optical routing elements, and optical detectors and their associated amplifiers in the output plane. The optical elements in the layer are used to route the input optical signals toward the output plane and achieve the required communication topology.

The power efficiency and the communication bandwidth achievable in a photonic layer are critical for enabling the pervasive use of optical interconnects between chips. Previous to this program, our modeling studies had revealed that FSOI can become a viable approach for implementing high speed (>1Gb/s per channel) and high density interchip communication channels only if the photonics layer could provide a higher bandwidth and consume an equal or less power than conventional electronic systems. With recent progress made in transmitter technologies, optical receivers have now become the performance limiting factor in an FSOI.

The primary thrust of this program was therefore to investigate new technologies for implementing high-performance receivers for (FSOI). Besides high bandwidth requirement (.5-2.5Gb/s), an optical receiver in FSOI applications must have significant gain to minimize the required optical power while satisfying the noise margins of electronic logic circuits. In addition, low electrical power dissipation is required to achieve an overall large aggregate bandwidth in a given area. Furthermore, the receiver design should be made area efficient. Unlike their counterparts for long haul telecommunication systems, the performance of optical receivers used in FSOI is limited by gain-bandwidth product rather than noise behavior. This is because the minimum input optical power to the receiver depends on the voltage requirement of the logic circuitry, rather than the receiver noise as in the case of optical fiber communication.

Thus amplification of the signals received at the destination become especially important to maintain power efficiency and bit error performance of the link. To amplify the signal prior to the receiver amplifier, one can use either optical amplifiers prior to the detection, or photodetectors with gain. Photodetectors with gain, such as avalanche photodiodes and phototransistors, have been investigated by many researchers for more than two decades. The concern in using avalanche photodiodes is gain stability and the required large bias voltage. Gain stability requires a rather extensive circuit to achieve good feed-back gain control. Implementing 2-D arrays of avalanche detectors remains, therefore, a difficult task. In addition, avalanche photodiodes require high operating voltages that increase the electrical power dissipation significantly at high operating frequencies. Phototransistors are basically an integrated version of photodiodes and bipolar transistors. The transistor structure has to be modified to accommodate photodetection. This results in a large collector junction and a reduced bandwidth.

Optical amplification is inherently fast, because the multiplication process takes place in the photon population rather than in the electron population. Optical amplifiers can be considered independent from electronic logic technologies. Consequently they can be used to complement any post detection amplifiers. It is with these considerations in mind that we performed the studies outlined earlier and described in greater details in appendices below.

Appendix I-Publications and Patent Applications

1. Van Blerkom, D.A., Kibar, O. and Esener, S.C., "Optical receivers optimized for IST and jitter," *Proceedings IEEE LEOS '97, 10th Annual Meeting,*.San Francisco, CA, USA, No.97CH36057, vol.1, p. 254-5, November 1997.
2. D.A. Van Blerkom, Fan, C., Blume, M., and Esener, S.C., "Transimpedance receiver design optimization for smart pixel arrays," *Journal of Lightwave Technology*, vol.16, no.1, IEEE, p.119-26, January 1998.
3. Kibar, O., Van Blerkom, D., Fan, C., P. J. Marchand, P.J., and Esener, S.C., "Small Signal Equivalent Circuits for a Semiconductor Laser," *Applied Optics 37*, pp. 6136-6139, September 1998.
4. Kibar, O.; Marchand, P.J.; Esener, S.C., "Gain-bandwidth product of a VCSEL amplifier", Conference Proceedings. LEOS '98. 11th Annual Meeting, Orlando, FL, USA, Piscataway, NJ, USA: IEEE,. p.221-2 vol.2, Dec. 1998
5. Kibar, O.; Van Blerkom, D.A.; Fan, C.; Esener, S.C., "Power minimization and technology comparisons for digital free-space optoelectronic interconnections", Journal of Lightwave Technology, vol.17, (no.4), IEEE, p.546-55, April 1, 1999
6. Kibar, O. Flynn, R.A., and Esener, S.C. "Spatial mode control of a midsize proton-implant VCSEL and its application to superresolution " ,OSA Topical Meeting on Spatial Light Modulators, Snowmass, April 1, 1999
7. Milbee, N.M., Kibar, O., and Esener, S.C.," Controlling the Polarization of Small-diameter VCSELs through Asymmetric Etch of the Bottom Mirror Perimeter," OSA Topical Meeting on Spatial Light Modulators, Snowmass, CO. April 14, 1999
8. Flynn, R., Kibar, O., and Esener, S.C., "Super-resolution by spatial filtering of high-order Laguerre-Gaussian mode VCSELs," Joint International Symposium on Optical Memory and Optical Data Storage, Koloa, Hawaii, July 11, 1999
9. Flynn, R.A.; Kibar, O.; Hartmann, D.; Esener, S.C., "Superresolution using a vertical-cavity surface-emitting laser (VCSEL) with a high-order Laguerre-Gaussian mode," Japanese J. Appl. Phys, Part 1 vol.39, (no.2B), p.902-5, February 1, 2000
10. Wen, P., Sanchez, M., Kibar, O., Esener, S.C., "Low-voltage, high contrast-ratio, low-noise VCSEL modulator," OSA topical meeting on Optical Amplifiers and Their Applications, Quebec City, Canada, July 1, 2000

Patent Applications

Esener, S.C., Kibar, O., "New High Performance Optical Super-resolution Technique" UC#1999-035

Esener, S.C., Kibar, O., "Ultra-Low Voltage, High Contrast Ratio, High Speed Spatial Light Modulator" UC#1999-075

Appendix II:

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3. Osman Kibar	Junior Partner Pequot Ventures (New York) Co-founder of Genoptix Inc.

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Appendix III: Receiver modeling and optimization

Receiver sensitivity, speed, power consumption, and area requirements are critical to the design of opto-electronic ICs. In this Appendix III, we present a receiver model and an optimization methodology that enables the design of optimal receivers. We have shown that the receiver sensitivity is limited by the gain-bandwidth product of the receiver amplifiers and the minimum noise margin required at the logic circuits. The method for minimizing the total power, including the electrical power of the receiver and the transmitter, yields an increase in the required optical power at the receiver and a decrease in the total power dissipation. This is important, as the effective area of a receiver due to power density considerations will be larger than the actual layout area. Our approach is not limited to CMOS based receivers. With a complete description of the amplifying stage gain, bandwidth, and capacitances, a similar optimization can be done for other technologies.

Optical receiver circuits for FSOI are typically mixed mode circuits with an analog front end and a digital decision making circuit. To properly analyze analog circuits, it is important to have a reasonably accurate mathematical model of MOSFET performance. On the other hand, a model with an excessive number of parameters is intractable for hand analysis and fast computer simulations, as well as obscuring the physical processes involved. Modern sub-micron SPICE or HSPICE models require more than 50 parameters to model a MOSFET in all of its possible regions of operations. Models which use binning so that different parameters can be used for different device dimensions require even more. Unfortunately, even with this huge number of parameters these models often fail to accurately model device performance.

The MOSFET model that we have developed and used to optimize trans-impedance amplifiers for FSOI receivers is a simple one, designed to model devices in the saturation region of operation. It is based on models described in the literature, and includes the short-channel effects that dominate performance at sub-micron dimensions. It does not attempt to reproduce the accuracy of the more extensive models. However, the accuracy lost when using only a few parameters is often inconsequential, because the inherent accuracy is limited by CMOS process variations.

Optical receivers can be classified as high-impedance, transimpedance, and low-impedance, depending on the pre-amplifier design. When the timing of the optical signal is known, an integrate-and-dump pre-amplifier design can be used as well. The four receiver classifications are shown in Figure III.1.

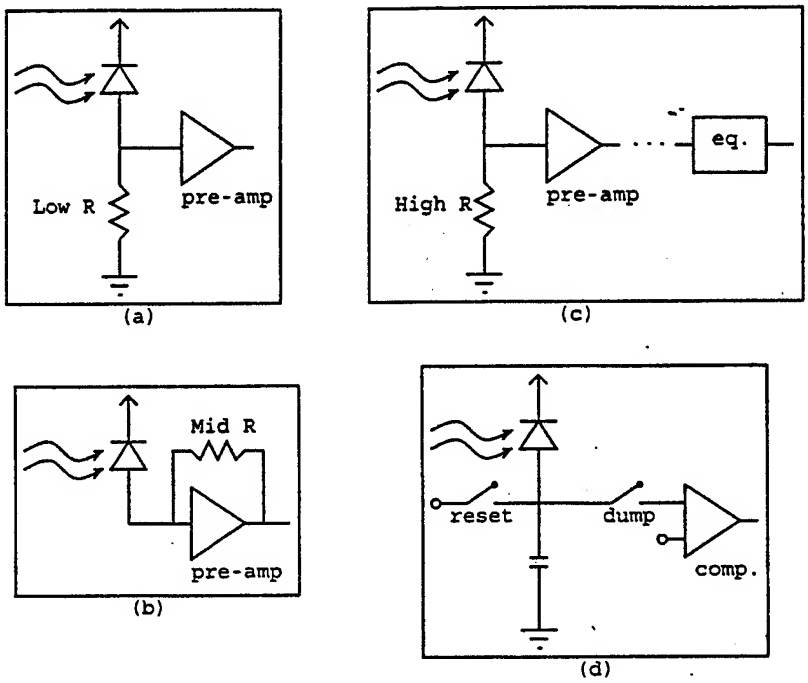


Figure III.1: Receiver classifications: (a) low impedance, (b) transimpedance, (c) high impedance, and (d) integrate-and-dump.

receivers have a broad bandwidth, but poor sensitivity. High-impedance receiver have much better sensitivity, but require some form of equalization to achieve a useful bandwidth. The transimpedance receiver, which uses negative feedback to broaden the bandwidth while maintaining a reasonable sensitivity, provides a good compromise between the two extremes. In addition, the use of feedback self-biases the pre-amplifier to the high-gain region of operation. This chapter assumes a transimpedance receiver design.

The integrate-and-dump pre-amplifier can potentially provide much better sensitivity than all of the other pre-amplifiers. It does this by integrating the photocurrent on a capacitor over the entire bit-period, instead of directly converting the photocurrent to a voltage. A comparator can then be used to decide if the integrated charge represents a one or zero bit. This is the principle of operation for the clocked sense-amplifier based receivers discussed by Woodward in [55].

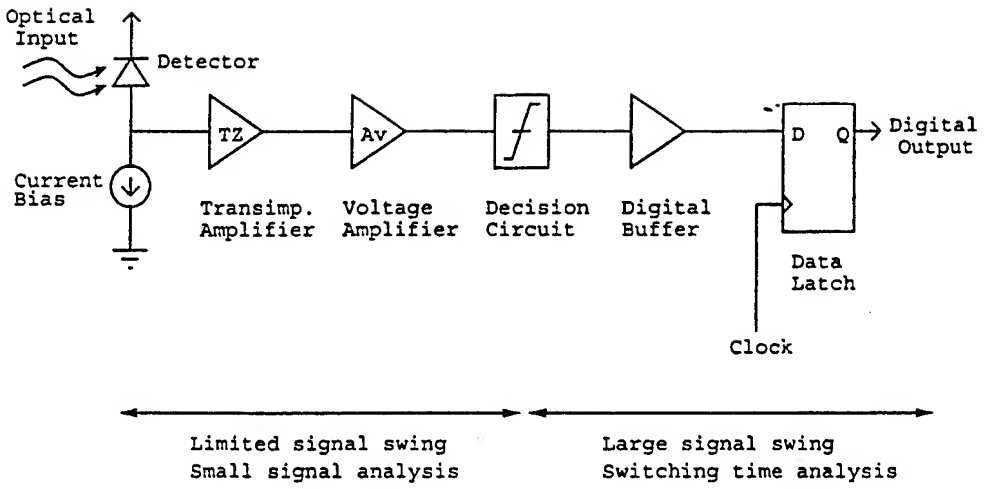


Figure III.2: Transimpedance receiver block diagram.

It has also been applied to electrical interconnects by Sidiropoulos and Horowitz [56]. However, these receivers must be reset before every bit, thus requiring either return-to-zero (RZ) signaling as in [55], or two interleaved pre-amplifiers as in [56]. In addition, precise timing information must be available to determine the integration period. These receivers are an area of continuing research.

The operational model of a transimpedance receiver can be broken into five components, as shown in Figure III.2 — the transimpedance amplifier (TIA), the voltage amplifier, the decision circuit, the digital buffer, and the data latch. The transimpedance amplifier converts the photo-current from the detector to an analog voltage. This voltage is then amplified by the voltage amplifier to match the requirements of the decision circuit. The decision circuit provides a digital voltage output to the following digital buffer. The latch then samples and re-synchronizes the receiver output to the local system clock. A current bias at the detector is used to provide an offset to the detector current. This is done so that the amplifier input swings around the bias point, which is set by the self-biasing action of the transimpedance amplifier to the point in the transfer curve where $V_{in} = V_{out}$ (Figure III.3). The current bias can be further increased to compensate

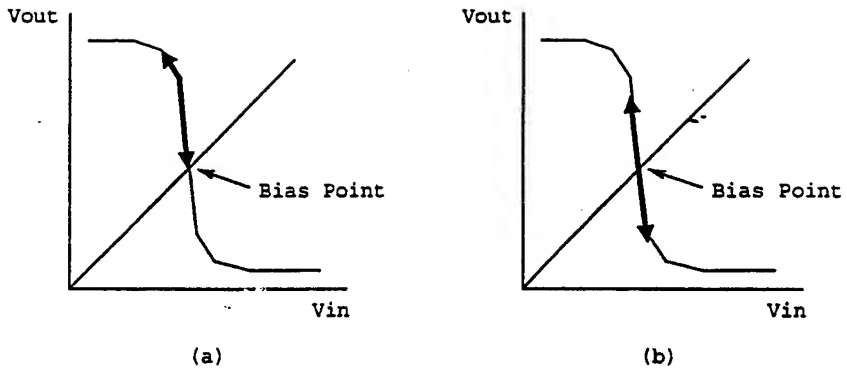


Figure III.3: Effect of the current bias on amplifier voltage swing (thick arrow): (a) without current bias and (b) with current bias (zero extinction ratio assumed).

for a non-zero extinction ratio (i.e. optical power is present when transmitting a zero).

The analysis of the receiver is separated into two regimes, as shown in Figure III.2. From the photodiode to the decision circuit, the voltage swings are relatively small, and a small-signal analysis can be used. From the decision circuit to the data latch, the voltage swings are at typical digital levels, and a switching time analysis is more appropriate.

In this chapter, no coding of the signal is assumed. Without a DC balanced code, the receiver components must be DC coupled, and the decision threshold cannot be derived from the signal but must be generated internally. DC coupling also implies that the DC bias conditions must be the same for all the amplifying stages. In addition, because of the large size and performance-limiting parasitics of on-chip inductors, this analysis does not include designs with inductive peaking. A separate optimization of inductive peaking in optical receivers is described in [57].

III.C.1 Gain stage

A transimpedance receiver can include many amplification stages, in both the TIA and the voltage amplifier. A fundamental issue in designing a receiver is the choice of the gain stage circuit design. Since the stages are DC coupled, the bias points must be the same for all the stages. This ensures that the entire amplification chain will be biased in the high-gain region. For this reason, a given receiver's gain stages are all chosen to be identical in this study.

Gain stage options

Basic gain stage designs are depicted in Figure III.4. A detailed analysis of these gain stages can be found in standard textbooks on analog design (e.g. [58]), and is summarized here. The amplifiers are assumed to be biased at $V_{in} = V_{out}$. The simplest possible design is a CMOS inverter (Figure III.4(a)), which requires no bias voltages and only two transistors. This gain stage has the highest gain-bandwidth product when driven by a ideal voltage source, but this is partially offset by the larger input capacitance due to the PMOSFET when driven from a high impedance source. The gain is not very adjustable by the designer, as the bias current cancels out to first order in the gain equation. In addition, the gain is sensitive to process variations, as it depends on both NMOS and PMOS parameters. Another problem is that the gain falls off rapidly around the bias point, limiting the valid region of the small-signal analysis. The stage also swings from rail to rail, which is of course one reason it is preferred for digital circuits. For a receiver, however, a gain stage with a large output swing can reduce the dynamic range by slowing down the receiver when it is operated with a larger input optical power than the minimum required optical power. This is due to the limited slew rate of the amplifier when it is operated beyond the small-signal limits.

The next simplest stage is the current-source inverter (Figure III.4(b)), which replaces the signal voltage on the PMOSFET with a constant bias voltage. This stage can have a lower input capacitance than the CMOS inverter, but since

the transconductance of the PMOSFET is not used it also has a smaller gain. However, the bias voltage gives more freedom to adjust the gain of the stage, which can be tuned over a relatively wider range than that of the CMOS inverter. In addition, with proper biasing the power supply rejection ratio of this gain stage can be improved over that of the CMOS inverter, as discussed in Section III.D.9.

Both of these designs suffer from the Miller effect, which multiplies the parasitic capacitance between the gate and drain of the input MOSFET by the gain. This effect is avoided when using a cascode design (Figure III.4(c) & (d)). The cascode transistor, which is basically a common gate amplifier, also greatly increases the gain at the expense of bandwidth. However, the gain in this case cannot be determined very accurately, as the inaccuracies in the modeled output conductance are effectively squared by the cascode action. In addition, the parasitic capacitance of the additional transistor lowers the gain-bandwidth of these amplifiers to below that of the non-cascode amplifiers. Other disadvantages are the multiple bias voltages required, and poor performance at smaller power supply voltages due to the extra voltage drop required across the cascode transistor.

The gain stage design used in the receivers described here is the ratioed current-source (RCS) inverter, and is shown in Figure III.4(e). This gain stage is also called a current-steering amplifier (CSA) in [59], which describes its use in a PLL design. This gain stage is based on the current-source inverter (FETs M1 and M2), but includes an additional diode-connected transistor (M3) at the output. M3 serves to shift the output pole to higher frequencies, by reducing the small-signal impedance on the inverter's output node; it also simultaneously reduces the gain of the inverter. This allows more precise control over the gain and bandwidth of the stage, which is critical to determining the receiver's transfer function. The maximum output swing of the RCS inverter is reduced from that of the other inverters, which as previously mentioned can increase the dynamic range of the receiver. This gain stage circuit, or a similar design where the current-source inverter is replaced with a CMOS inverter, has been used in prior GaAs and CMOS

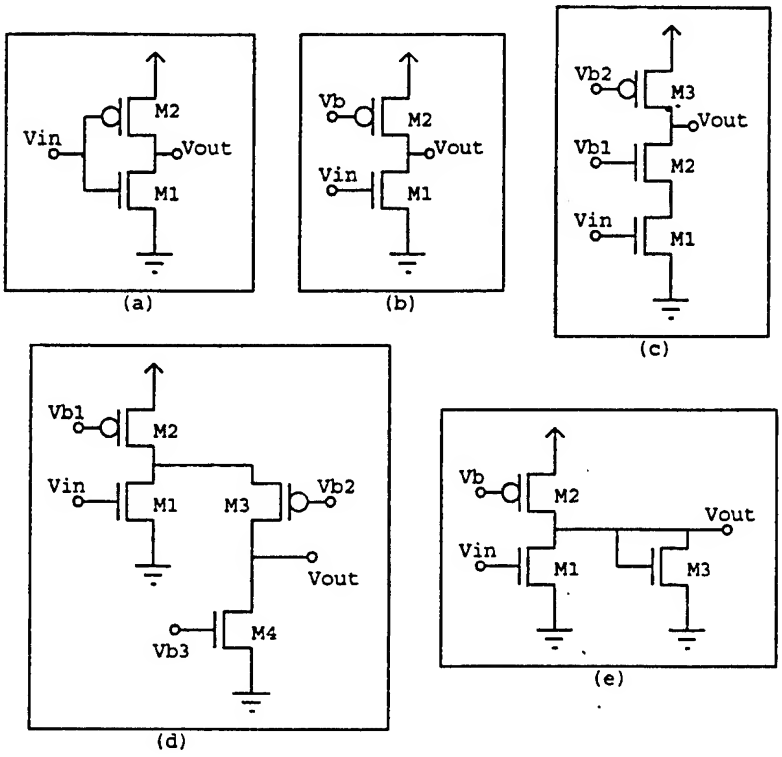


Figure III.4: Gain stage circuit designs: (a) CMOS inverter, (b) current-source inverter, (c) telescopic cascode, (d) folded cascode, (e) ratioed current-source inverter

OEIC receivers [24],[40]. High gains can be obtained from this low-gain stage by simply cascading the stages.

Figure III.5 compares the gain variation for a CMOS inverter and a RCS inverter across 11 runs of 0.5 μm CMOS from MOSIS. The two gain stages were designed to have the same bias power dissipation. Also shown on the graphs is a gaussian fit to the gain distributions. The RCS inverter's gain is more tightly controlled than that of the CMOS inverter. This also means the RCS inverter has a more precisely defined input capacitance, because the Miller effect depends on the gain.

Figure III.6 demonstrates how much more adjustable the gain of the RCS

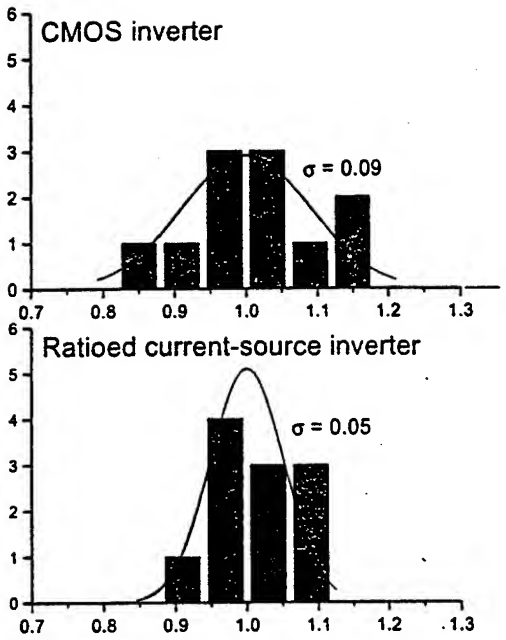


Figure III.5: Normalized gain variation for the CMOS inverter and the RCS inverter across eleven 0.5 μm MOSIS runs. The RCS inverter has a smaller variation across process variations.

inverter is compared to that of the CMOS inverter. By varying the bias voltage V_{gs} and transistor size W_1, the gain of the RCS inverter can be tuned over a wide range. In comparison, the CMOS inverter's gain is relatively constant over changes in V_{gs} and W_1.

RCS inverter design

Having chosen the RCS inverter as the fundamental gain stage, an analysis of its performance can be developed. Referring to Figure III.4(e), the output voltage and the input voltage are the same when biased in the high gain region, $V_{in} = V_{out} = V_{gs}$. The bias voltage V_b on M2 is chosen to be the same as its

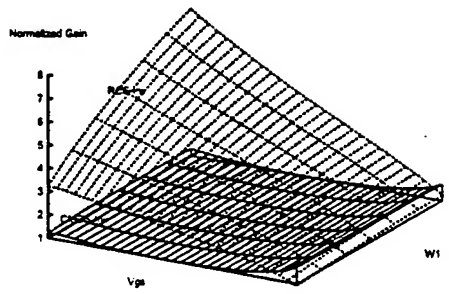


Figure III.6: Normalized gain versus V_{gs} and W_1 for the CMOS inverter and the RCS inverter in 0.5 μm CMOS. Unlike the CMOS inverter, the RCS inverter's gain is adjustable over a wide range.

Table III.1: Gain stage comparison

Gain Stage	Gain	Bandwidth	Accuracy
CMOS inverter	med	high	poor
Current-source inverter	low	high	poor
Telescopic cascode	high	low	bad
Folded cascode	high	low	bad
Ratioed current-source inverter	low	high	good

bias drain voltage, V_{gs}, to ensure that it remains in saturation. The gain of the corresponding current-source inverter (i.e. Figure III.4(b)) is given by:

$$A_0 = \frac{g_{m1}}{g_{ds1} + g_{ds2}} \tag{III.1}$$

Using the equations for the MOSFET small-signal characteristics (Equations II.2 and II.4), it can be seen that this gain depends only on the gate-source voltage of M1. Changing the value of W_1 changes the bias current but does not alter the gain. However, when the effect of M3 is taken into account, the transconductance of M3 adds to the output conductances in the denominator of Equation III.1. This means the ratio of W_1 to W_3 becomes important. Small values of this ratio correspond to low gain, high speed amplifiers, whereas larger values corre-

spond to higher gain, lower speed amplifiers. The gain is calculated to be

$$A_v = g_{m1} R_o = \frac{W_1}{W_3 + (W_1 + W_3) A_0^{-1}} \qquad \text{(III.2)}$$

where Ro is the output resistance given by

$$R_o = \frac{1}{(g_{ds1} + g_{ds2} + g_{ds3} + g_{m3})} \qquad \text{(III.3)}$$

Note that for large values of A_0, the gain becomes simply the ratio of the two widths, $\frac{W_1}{W_3}$. In this ideal case, the gain would be set by the geometry of the design, and would not depend on the transistor characteristics. Unfortunately, the value of A_0 is typically not large enough to make the additional terms in Equation III.2 negligible, although it does improve the performance with respect to parameter variations, as shown previously in Figure III.5.

If this gain stage is the last or only stage in the TIA, it has a feedback resistor at its output. This feedback resistor lowers the gain of the amplifying stage it loads. Taking into account the effect of the feedback resistor, the loaded gain A'_v is given by:

$$A'_v = \frac{A_v R_f - R_o}{R_o + R_f} \qquad \text{(III.4)}$$

The input and output capacitances of the amplifying stage can be written

$$C_{in,amp} = C_{gsw} W_1 \qquad \text{(III.5)}$$

$$C_{f,amp} = C_{gow} W_1 \qquad \text{(III.6)}$$

$$C_{in,amp,miller} = [C_{gsw} + C_{gow}(1 + A_v)] W_1 \qquad \text{(III.7)}$$

$$C_{out,amp} = C_{jw} W_1 + (C_{gow} + C_{jw}) W_2 + (C_{gsw} + C_{jw}) W_3 \qquad \text{(III.8)}$$

where the second term in Equation III.7 is due to the Miller effect. The width of M2 can be determined by equating the currents in the P and N channel

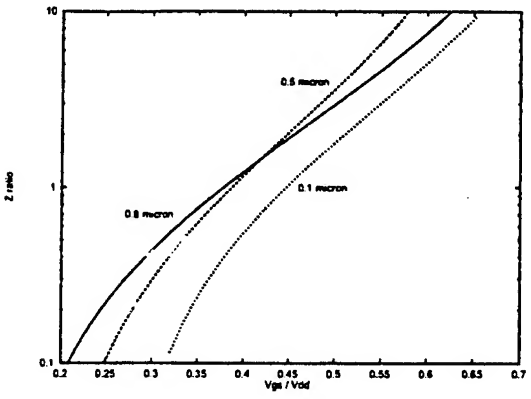


Figure III.7: Z ratio vs. V_{gs}/V_{dd} for three CMOS processes.

devices, and is given by $W_2 = Z(W_1 + W_3)$, where Z is (using Equation II.1):

$$Z = \frac{\beta_n (V_{gs} - V_{tn})^2 \left[1 + \theta_p \left(V_{dd} - V_{gs} - V_{tp}\right)\right]}{\beta_p (V_{dd} - V_{gs} - V_{tp})^2 \left[1 + \theta_n \left(V_{gs} - V_{tn}\right)\right]} \tag{III.9}$$

Figure III.7 plots the value of Z versus V_{gs}/V_{dd} for the three CMOS processes described in Section II.A. Z varies from approximately 0.1 at $V_{gs} = 0.2V_{dd}$ to 10 at $V_{gs} = 0.7V_{dd}$, for all three processes. The curve for 0.1 μm CMOS is offset to the right due to the larger V_t/V_{dd} ratio in this process, which arises from the difficulty in scaling the threshold voltage as mentioned in Section II.A.

The pole at the output of the amplifying stage determines its 3-db bandwidth. This pole can be written,

$$f_{-3db} = \frac{1}{2\pi R_o \left(C_{out,amp} + C_{next}\right)} \tag{III.10}$$

If this stage is loaded with a feedback resistor, it will act in parallel with the output resistance, moving the pole to:

$$f'_{-3db} = f_{-3db} + \frac{1}{2\pi R_f \left(C_{out,amp} + C_{next}\right)} \tag{III.11}$$

C_{next} in (III.10) and (III.11) is the input capacitance of the next amplifying stage, $C_{in,amp,miller}$, or the input capacitance of the decision circuit, C_{dc}, if this is the last stage in the receiver. Thus, given the CMOS process parameters,

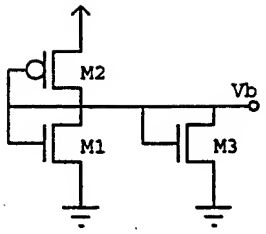


Figure III.8: Gain stage voltage bias generator.

the gain and bandwidth of the RCS inverter can be written in terms of W_1 and V_{gs} (and R_f if necessary).

The gain stage voltage bias V_b can be generated from an additional gain stage by tying its input and output together, as shown in Figure III.8. If a lower output resistance is required from the bias generator, several stages can be used. Capacitive de-coupling of the voltage bias can also be used to keep the shared voltage bias line from providing positive feedback which would lead to oscillations. De-coupling is discussed in Section III.D.9.

III.C.2 Feedback resistor

A feedback resistance is required in the transimpedance amplifier, as shown in Figure III.16. Unfortunately, the fabrication of high quality resistors in standard CMOS is difficult. Unsilicided poly-silicon can be used (if the silicide blocking option is available), but the sheet resistance of the poly is still low, around 150 ohms/square. This means that the parasitic capacitance for large resistance values severely limits the receiver speed, as well as requiring a large layout area. The best option for small parasitics is to use small MOSFETs operating in the linear region.

The implementation of the feedback resistor in this analysis is shown in Figure III.9. The circuit consists of a NMOS and PMOS transistor connected in parallel. The PMOS gate is controlled by a tunable voltage V_{pfb}, while the NMOS gate is controlled by a tunable voltage V_{nfb}. The PMOS well is tied to the bias

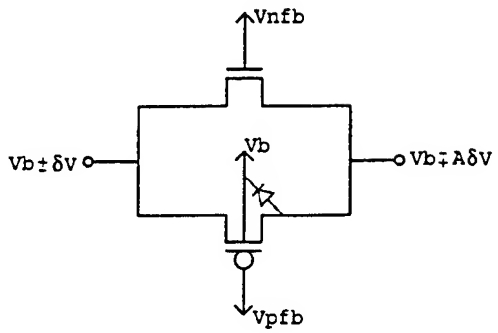


Figure III.9: Feedback resistor implementation.

voltage V_b to reduce the impact of the body effect. The transistor sizes are chosen as small as possible in both width and length to reduce the junction parasitics and the channel charge.

This complementary design for the feedback resistor is used to attempt to reduce the non-linearity caused by the asymmetry of the voltage swing across the resistor terminals. The terminal connected to the input of the TIA varies by δV around V_b, whereas the terminal connected to the TIA output varies by $A\delta V$, where A is the voltage gain of the TIA. This means that the NMOS transistor will be turned on to a greater extent when the output of the transimpedance amplifier is low versus when it is high. The PMOS transistor balances this trend by turning on when the transimpedance amplifier output is high.

Figure III.9 also shows the source-well junction diode on the PMOS transistor. Because the well of the PMOSFET is tied to V_b, the diode will conduct when a voltage larger than a diode drop above V_b appears at the output of the TIA. The diode is not conducting during normal operation, because the output swing of the TIA is not required to reach this forward turn-on voltage. However, when the TIA is over-driven the diode provides a current path that limits the output swing. This limiting effect can extend the dynamic range of the receiver by reducing internal voltage swings when the input optical power is larger than required. Note, however, that the junction capacitance seen at both the source

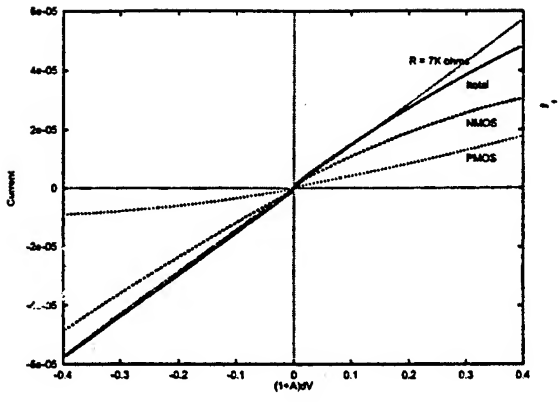


Figure III.10: Current through a feedback resistor versus voltage drop across it. The resistance was designed to be $7K\Omega$. The contributions from the NMOS and PMOS devices are shown.

and drain of the PMOSFET is larger than if the well were tied to V_{dd}, due to the reduced voltage drop across the junctions.

Figure III.10 shows the contributions from the NMOS and PMOS devices for a $7K\Omega$ feedback resistance and a gain of $A = 10$. Note that when a voltage amplifier is used after the TIA, the required output swing from the TIA is smaller, and much better linearity can be achieved.

III.C.3 Decision circuit

The decision circuit is chosen to be a current-source inverter (Figure III.4(b)) instead of a RCS inverter. This is because a precise gain is not required in the decision circuit, and the RCS inverter's limited voltage output swing is not appropriate for the decision circuit, which must produce digital logic level outputs. The ratio of the PMOS to NMOS width in the current-source inverter is calculated to make the inverter switching voltage the same as the bias voltage V_b. This ensures that both transistors are in the saturation region at the switching point. This ratio is given by the parameter Z defined in Equation III.9.

The operation of the decision circuit is non-linear, and a small-signal

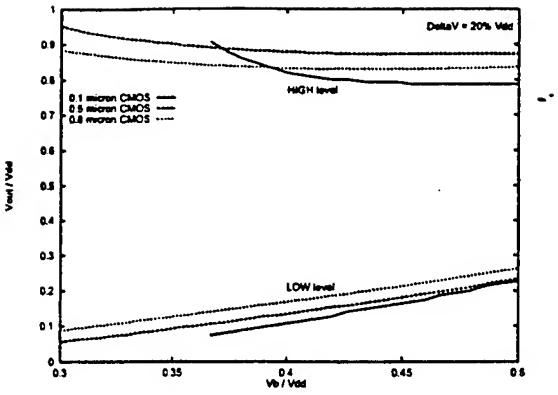


Figure III.11: Decision circuit output levels versus switching voltage for three CMOS processes. The input voltage swing is from $V_b - 10\%V_{dd}$ to $V_b + 10\%V_{dd}$.

analysis is not applicable. A minimum voltage swing, ΔV, must be input to the decision circuit to ensure an adequate output swing. This input voltage swing is the width of the voltage transition region of the decision circuit.

The width of the transition region for the decision circuit is given approximately by $\Delta V \approx 20\%V_{dd}$. Using this value of ΔV, the output levels of the decision circuit are shown in Figure III.11 for different values of V_b. Each value of V_b corresponds to a different design ratio of PMOS to NMOS width. Note that as V_b increases the NMOS size decreases. This reduces the pull-down ability of the NMOS device, thus allowing the low output level to rise. However, with the given ΔV the output swing is at least $60\%V_{dd}$ for all values of V_b. If the following Schmitt trigger also has a transition region width of $20\%V_{dd}$ around $V_{dd}/2$, then this output swing is large enough to switch the Schmitt trigger and provide a margin of $20\%V_{dd}$ on either side for reliable operation in the presence of noise and parameter variations. Of course, special care must be taken to avoid digital switching noise from entering the small-signal part of the receiver, as there is no such noise-margin there. This is discussed further in Section III.D.9.

The ratio of the PMOS to NMOS width is set by V_b, but the absolute values of the widths are determined by the required switching speed. If large widths

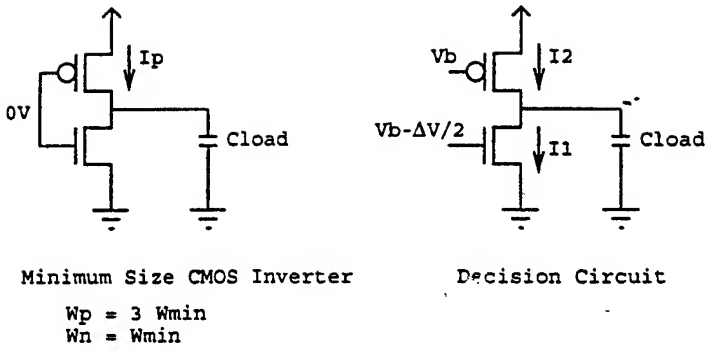


Figure III.12: The decision circuit output rise time is made equal to that of a minimum sized CMOS inverter by setting the width of W2 such that $I_2 - I_1 = I_p$.

are chosen, the decision circuit will be able to switch its load capacitance quickly, but will present an unacceptably large load to the receiver amplifier and thus slow it down. On the other hand, if the devices are undersized, then the decision circuit becomes the speed limiting circuit in the receiver. To analyze the affect of the decision circuit, its speed must be characterized in terms of the transistor widths.

The decision circuit rise time is typically slower than its fall time, due to the smaller pull-up strength of the PMOS transistor. In order to develop an equation for the decision circuit rise time, we first find the condition where the rise time is equal to that of a minimum sized CMOS inverter (with PMOS width $W_p = 3W_{min}$ and NMOS width $W_n = W_{min}$). The initial charging currents when the input is switched from high to low are set equal by an appropriate choice of W_2:

$$I_2 - I_1 = I_p \tag{III.12}$$

where I_p is the inital charging current of the PMOSFET in the CMOS inverter (with $V_{gs} = V_{dd}$), I_2 is the charging current through M2 ($V_{gs,2} = V_{dd} - V_b$), and I_1 is the discharging current through M1 ($V_{gs,1} = V_b - \frac{\Delta V}{2}$). These currents are shown in Figure III.12. The width of M2 (and thus of M1 through the factor Z) is chosen to solve Equation III.12. Figure III.13 shows the values of W_1 and W_2

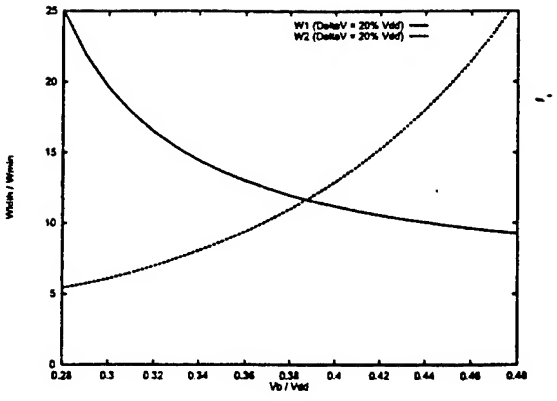


Figure III.13: Decision circuit transistor widths which produce a rise time equal to that of a minimum sized CMOS inverter. Widths are in terms of W_{min} for the 0.5 μm CMOS process. Curves are shown for W_1 and W_2, for $\Delta V = 20\%V_{dd}$.

versus V_b for the 0.5 μm CMOS process.

The rise time of the decision circuit can thus be written in terms of the rise time of a minimum sized CMOS inverter, as:

$$t_r = 2.2\tau_{min}\left(\frac{I_p}{I_2 - I_1}\right)\left(1 + \frac{C_{next}}{C_{min}}\right) \qquad \text{(III.13)}$$

C_{min} is the input capacitance of a minimum sized inverter and τ_{min} is the RC time constant of a minimum sized inverter, as given in Section II.B.

III.C.4 Digital Buffer

The first stage of the digital buffer is a small CMOS Schmitt trigger. This is followed by a cascade of CMOS inverters, starting with a minimum-sized inverter and scaling upwards in size by a constant factor g (Figure III.14). This super-buffer arrangement presents a small load capacitance to the decision circuit, while the super-buffer output drive capability can be increased by adding additional scaled stages.

The ratio of input transistor width to feedback transistor width in the Schmitt trigger is chosen to give a hysteresis loop with a width V_{hyst} of approximately $20\%V_{dd}$ around $V_{dd}/2$. This ratio is given by [60]:

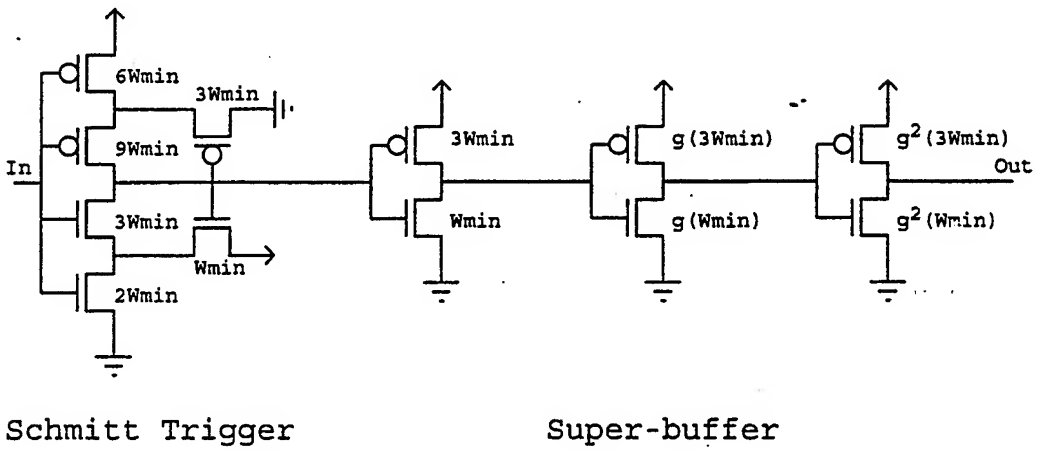


Figure III.14: Digital buffer.

$$\beta_r = \left(\frac{V_{dd} - V_{hyst}}{V_{dd} + V_{hyst} - 2V_t}\right)^2 = \left(\frac{1 - 0.2}{1 + 0.2 - 2(0.3)}\right)^2 \approx 2 \qquad \text{(III.14)}$$

A minimum transistor is chosen as the NMOS feedback transistor, and the two NMOS input transistors are sized at 2 and 3 times the minimum width. The PMOS transistors are sized 3 times larger than the corresponding NMOS transistor. Using the transistor widths shown in Figure III.14, the input capacitance of the Schmitt trigger can be written in terms of the input capacitance of a minimum sized inverter (C_{min}). This input capacitance is approximately $5C_{min}$.

The Schmitt trigger circuit is included to suppress oscillations due to unintended feedback from the super-buffer into the receiver amplifiers and decision circuit. By adding this hysteresis to the digital buffer, the switching of the super-buffer does not occur when the decision circuit is in its highest gain region of operation. This and other sources of instability are discussed further in Section III.D.9.

The final super-buffer stage drives the latch capacitance C_{latch}. Expressions for the propagation delay and output rise time of the super-buffer are given in Section II.B. The number of stages is chosen to minimize the propagation delay, while maintaining a fast enough edge rate such that the data input to the data

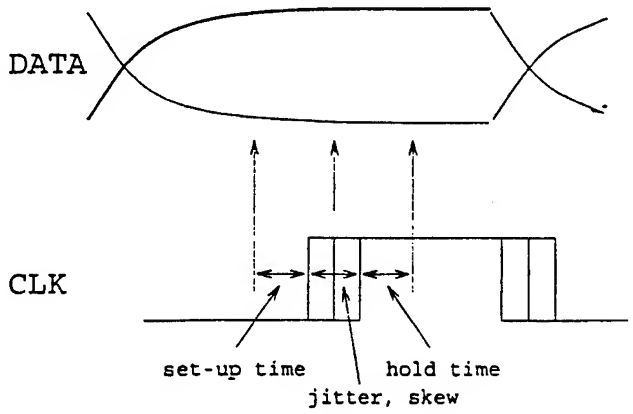


Figure III.15: Timing margin for data latch, including jitter and skew.

latch is stable around the clock edge. This depends on the input capacitance of the data latch, C_{latch}.

III.C.5 Data Latch

The last component of the receiver is the data latch. The latch samples the output of the digital buffer at the rising edge of the system clock. The sampled value is stored until the next rising edge. This allows the incoming data to be resynchronized to the local clock. The latch has an input capacitance of C_{latch}. The data must be stable at the input of the latch for a set-up time t_{setup} before the clock edge, and a hold time t_{hold} after the clock edge. The clock edge is nominally aligned with the center of the received bit, although jitter and skew in the clock and the data will cause the sampling point to move. The total timing margin over which the data should be stable is shown in Figure III.15.

III.D Receiver Model

Using the analysis for the receiver building blocks from the previous section, the full receiver model can be developed. The transimpedance amplifier is designed for stability by choosing an appropriate amount of feedback. The total

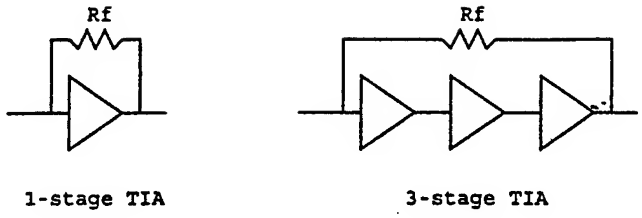


Figure III.16: Circuit for 1-stage and 3-stage transimpedance amplifier.

transimpedance and bit-rate of the receiver can then be calculated, as well as the input equivalent noise, electrical power dissipation, and circuit size, given the receiver configuration. The receiver configuration is coded as N+P, where N is the number of stages in the transimpedance amplifier, and P is the number of stages in the voltage amplifier.

III.D.1 Transimpedance Amplifier

The transimpedance amplifier (TIA) converts an input current to an output voltage. A feedback resistor R_f determines the transimpedance, and thus the sensitivity of the amplifier. Larger feedback resistors increase the sensitivity of the amplifier, but simultaneously reduce the amplifiers bandwidth. The bandwidth of the amplification stages that make up the TIA limit the ultimate speed of the TIA.

Both one-stage and three-stage TIAs are considered in this study, and are shown in Figure III.16. Note that the TIA must have an odd number of stages, so that the feedback is negative. For stability, an often used design goal is to make the transfer function of the feedback amplifier "maximally-flat." This corresponds to no peaking in the frequency response, and a slight overshoot in the time domain step response of 4.3%. For a transfer function with two dominant poles, the maximally flat condition is when the two poles are complex conjugates, and located at 45° from the axes in the left half s-plane (Figure III.17).

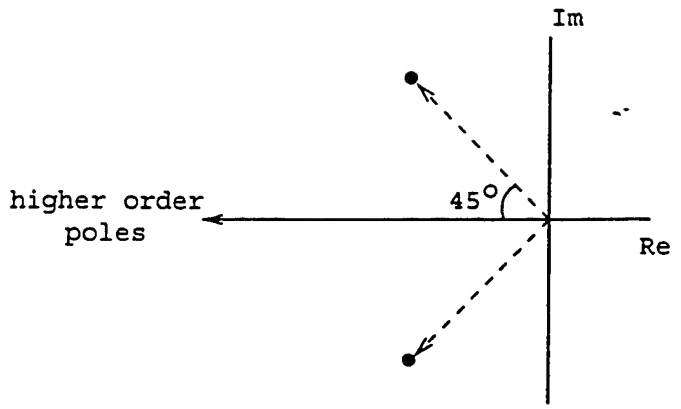


Figure III.17: Dominant pole locations in the s-plane for the maximally flat magnitude frequency response, with two poles.

One-stage TIA

The appropriate feedback resistor value to achieve a maximally-flat magnitude response from a transimpedance amplifier can be determined from its transfer function. The small-signal circuit diagram for the one-stage TIA is shown in Figure III.18. The corresponding transfer function can be written [23]:

$$Z_T(s) = \frac{A + sB}{C + sD + s^2E} \tag{III.15}$$

where the constants are:

$$A = R_o - A_v R_f \tag{III.16}$$

$$B = R_o R_f C_f \tag{III.17}$$

$$C = 1 + A_v \tag{III.18}$$

$$D = R_o(C_{in} + C_{out}) + R_f(C_f + C_{in}) + A_v R_f C_f \tag{III.19}$$

$$E = R_o R_f[(C_{in} + C_{out})C_f + C_{in}C_{out}] \tag{III.20}$$

and $A_v = g_m R_o$ is the unloaded open-loop voltage gain of the one-stage amplifier.

Note that in this section C_{in} is the input capacitance to ground of the amplifier and the photodiode capacitance, C_{out} is the total output capacitance to

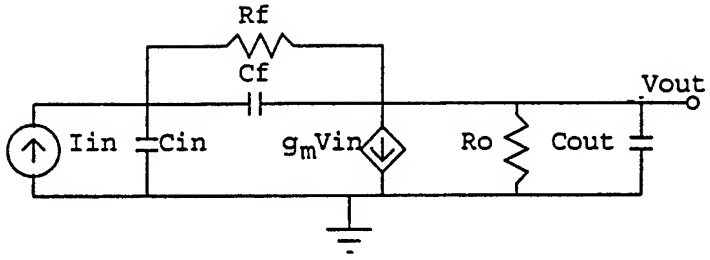


Figure III.18: Small signal circuit for the one-stage transimpedance amplifier.

ground of the amplifier plus the capacitive load of the next stage, and C_f is simply the amplifier feedback:

$$C_{in} = C_{pd} + C_{in,amp} \tag{III.21}$$

$$C_{out} = C_{out,amp} + C_{next} \tag{III.22}$$

$$C_f = C_{f,amp} \tag{III.23}$$

When the parameters for the gain stage are known, the location of the poles of the transfer function (Equation III.15) can be plotted as a function of the feedback resistor value. Figure III.19 is an example of this pole locus plot for a typical set of parameters. For large feedback resistances, the two poles are both on the real axis, and separated such that the pole at the input is clearly the dominant pole. As the feedback resistance reduces, the poles move toward each other until they merge. They then become complex conjugates, and move away from the real axis in opposite directions. They also move towards the left due to the broadbanding effect of the decreasing feedback resistance.

Also shown in this figure are the two 45° lines that mark the maximally flat pole positions. The intersection of these lines and the root locus indicate the feedback resistances that produce a maximally flat transfer function. In the figure, two solutions are shown. The first solution has smaller pole values, and is therefore slower than the second solution. On the other hand, the feedback resistance for the first solution is larger than that for the second solution. These tradeoffs are considered in the optimization procedure described in the next section.

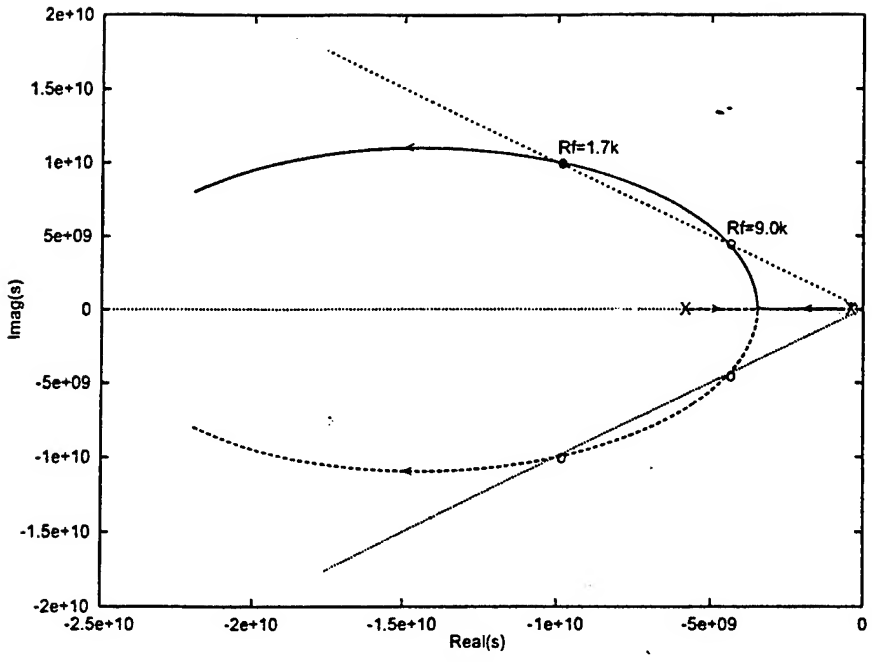


Figure III.19: Pole locus for a one-stage transimpedance amplifier as the value of R_f is changed. The intersection of the locus and the 45° lines marks the maximally-flat solutions. Note that there are two solutions in this example. Parameters used for the example are $g_m = 2.5mS, R_o = 4k\Omega, C_{in} = 140fF, C_{out} = 50fF, C_f = 5fF$. R_f varies from $10k\Omega$ (at the Xs) down to 600Ω.

Analytically, maximally-flat response of equation III.15 occurs when:

$$D^2 = 2EC \tag{III.24}$$

Solving equation III.24 leads to the following quadratic equation in R_f:

$$R_f^2[C_{in} + (A_v + 1)C_f]^2 + R_f[2R_oC_{in}(C_{in} - A_vC_{out})] + [R_o^2(C_{in} + C_{out})^2] = 0 \tag{III.25}$$

For convienence, define two capacitance ratios:

$$x = \frac{C_{out}}{C_{in}} \tag{III.26}$$

$$y = \frac{C_f}{C_{in}} \tag{III.27}$$

The normalized transfer function of the TIA can then be written, with ω measured in terms of α:

$$Z_t(\alpha \cdot \omega) = \frac{-2}{(\omega^2 + j\omega 2 - 2)} \tag{III.36}$$

If the simplified solution (Equation III.30) holds, then α can be written:

$$\alpha = A_v p_{in} = \frac{p_{out}}{2} \tag{III.37}$$

Thus two equations, III.33 and III.34, determine the sensitivity and speed of the one-stage transimpedance amplifier.

Three-stage TIA

Whereas the one-stage TIA has two poles, The three-stage TIA has four. The pole locus plot for the three-stage TIA is shown in Figure III.20, again for a typical set of gain stage parameters. The poles start at the "X"s for large values of R_f. There are three overlapping non-dominant poles, and one dominant pole to start with. As the feedback resistance decreases, two of the three non-dominant poles become complex conjugates and move toward higher frequencies. The dominant pole and one non-dominant pole move towards each other on the real axis, until they meet and become complex conjugates. These poles then move apart and to the right, eventually entering the right half plane at some small value of R_f. The intersection of the two inner poles with the 45° lines marks the maximally-flat solution. The figure also shows the position of the non-dominant poles at this solution point.

One important difference between the three-stage TIA and the one-stage TIA is the possibility for oscillation in the three-stage TIA, as evidenced by the dominant poles entering the right half plane. The proper choice for the feedback resistor is thus critical.

The transfer function of the three-stage TIA can be approximated:

$$Z_T(s) = \frac{R_f A_v^3(s)}{1 + A_v^3(s) + sR_f C_{in}} \tag{III.38}$$

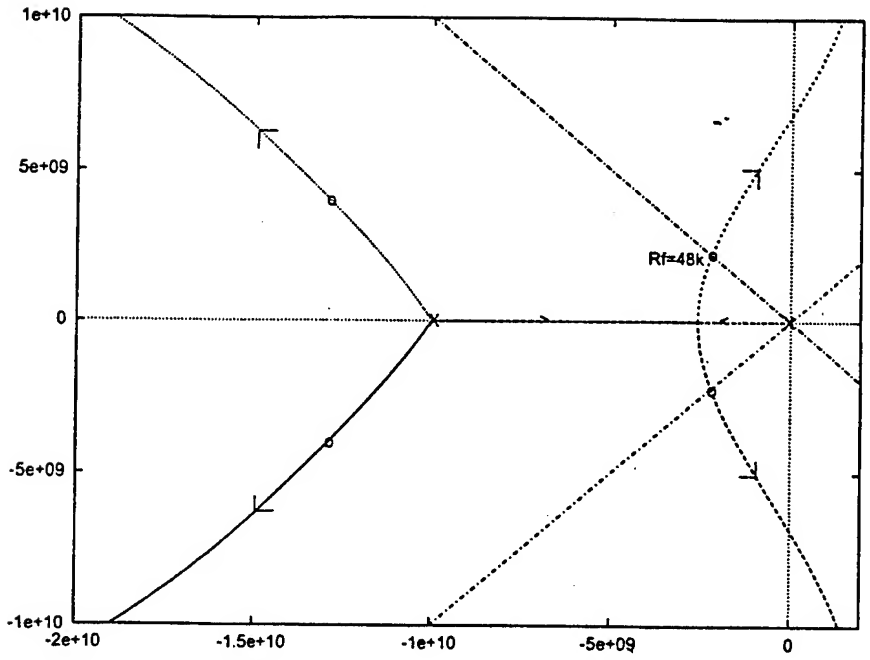


Figure III.20: Pole locus for a three-stage transimpedance amplifier as the value of R_f is changed. The intersection of the locus of the dominant poles and the 45° lines marks the maximally-flat solution. Also marked are the location of the non-dominant poles at this solution. Parameters used for the example are $g_m = 0.2mS, R_o = 10k\Omega, C_{in} = 105fF, C_{out} = C'_{out} = 10fF$. R_f varies from $10M\Omega$ (at the Xs) down to $1k\Omega$.

The first two of three stages in the TIA drive an output capacitance of C_{out}. The output capacitance of the third stage is C'_{out}, which may be different from the previous two stages if the TIA is connected directly to the decision circuit. The gain can then be written:

$$A_v^3(s) = \left(\frac{g_m}{R_o^{-1} + sC_{out}}\right)^2 \left(\frac{g_m}{R_o'^{-1} + sC'_{out}}\right) \tag{III.39}$$

where R'_o is the output resistance of the third stage, which is the parallel combination of R_o and the feedback resistance R_f.

$$R'_o = \frac{R_o R_f}{R_o + R_f} \tag{III.40}$$

Substituting Equation III.39 in Equation III.38, the full transfer function can then be written:

$$Z_T(s) = \frac{R_f A_v^3(0)}{A + sB + s^2C + s^3D + s^4E} \tag{III.41}$$

The terms are:

$$A = 1 + A_v^3(0) \tag{III.42}$$

$$B = 2R_oC_{out} + R'_oC'_{out} + R_fC_{in} \tag{III.43}$$

$$C = R_fC_{in}(2R_oC_{out} + R'_oC'_{out}) + R_oC_{out}(R_oC_{out} + 2R'_oC'_{out}) \tag{III.44}$$

$$D = R_fC_{in}(R_o^2C_{out}^2 + 2R_oC_{out}R'_oC'_{out}) + R_o^2C_{out}^2R'_oC'_{out} \tag{III.45}$$

$$E = R_fC_{in}R_o^2C_{out}^2R'_oC'_{out} \tag{III.46}$$

If the two sets of conjugate poles are far apart, then MFM response will occur when $B^2 = 2CA$. Assume that R_f is large enough so that $R'_o = R_o$, and that $C_{in} > C_{out}$, such that $R_fC_{in} \gg R_oC_{out}$. R_f can then be approximated as:

$$R_f = \frac{2R_oA_v^3(2C_{out} + C'_{out})}{C_{in}} \tag{III.47}$$

In terms of the input poles and output poles, this means (with the simplifying assumption that $C_{out} = C'_{out}$) :

$$p_{out} = 6A_v^3p_{in} \tag{III.48}$$

where the input and output poles are:

$$p_{in} = \frac{1}{R_fC_{in}} \tag{III.49}$$

$$p_{out} = \frac{1}{R_oC_{out}} \tag{III.50}$$

We have made the assumption that the feedback capacitance across the three stages is negligible and the feedback resistance is much larger than the output resistance, both of which are reasonable assumptions for the three-stage TIA. However, for accuracy, the optimization program described later solves for the pole locations numerically, using the equations given above for A through E.

Proceeding as before, the low-frequency transimpedance of the three-stage TIA is found from Equation III.38 to be:

$$Z_f = \frac{R_f}{1 + A_v^{-3}} \tag{III.51}$$

and the 10%-90% risetime of the three-stage TIA, when the transfer function is maximally flat, is

$$t_r = \frac{2.2\sqrt{2}}{2\alpha} \tag{III.52}$$

where the two inner poles are located at $p_{1,2} = -\alpha \pm i\alpha$.

The location of the poles can be found by using Equation III.48 in Equation III.41. After simplifying, this yields the equation for the denominator:

$$1 + x + \frac{x^2}{3} + \frac{x^3}{12} + \frac{x^4}{216} = 0 \tag{III.53}$$

$$x = \frac{s}{A_v^3 p_{in}} \tag{III.54}$$

Using the roots of this equation gives the the value of α as

$$\alpha = 1.25 A_v^3 p_{in} = \frac{p_{out}}{4.8} \tag{III.55}$$

The non-dominant poles are approximately

$$(-7.75 \pm i2.42) A_v^3 p_{in} = (-6.2 \pm i1.94)\alpha \tag{III.56}$$

The normalized transfer function of the TIA can then be written, with ω measured in terms of α:

$$Z_t(\alpha \cdot \omega) = \frac{84.4}{(\omega^2 + j\omega 12.4 - 42.2)(\omega^2 + j\omega 2 - 2)} \tag{III.57}$$

III.D.2 Voltage Amplifier

The voltage amplifier consists of a cascaded series of amplifying stages. As mentioned previously, the stages are all identical and use the same design as the stages in the transimpedance amplifier, to ensure proper DC biasing. The total gain provided by a P-stage cascaded voltage amplifier is thus A_v^P, where A_v is the gain of a single stage as defined in Section III.C.1.

One important consideration in the voltage amplifier is the effect of parameter variations on the DC biasing. Small variations in the transistor parameters can cause offsets that are amplified by subsequent stages in the amplifier, such that later stages may no longer be biased correctly. This problem is alleviated somewhat by the use of feedback in the TIA, but it must be taken into account in the voltage amplifier. Typical offsets between identical transistors in modern CMOS processes are in the 10 mV range. Since the gain of the amplifying stages is typically between 3 and 5, the maximum number of stages in the voltage amplifier is limited to two to keep the offset at the output of the voltage amplifier below 250 mV. This insures that all stages are correctly biased and that the input to the decision circuit swings about the threshold point. Although the offset improves slightly for smaller line-length technologies, the voltage swing reduces as well, indicating that the two stage limit is a reasonable choice for all three technologies considered [3].

The pole at the output of the voltage amplifier stage is at $p_{out} = \frac{1}{R_o C_{out}}$. Putting this in terms of α used above for the transimpedance amplifier poles means $p_{out} = 2\alpha$ for the 1-stage TIA, and $p_{out} = 4.8\alpha$ for the 3-stage TIA. Thus, the 10%-90% risetime of each stage in the voltage amplifier is:

$$t_r = \frac{2.2}{2\alpha} \tag{III.58}$$

for the 1-stage TIA, and

$$t_r = \frac{2.2}{4.8\alpha} \tag{III.59}$$

for the 3-stage TIA.

The normalized transfer function of the VA can then be written, with ω measured in terms of α:

$$Z_t(\alpha \cdot \omega) = \frac{j2^p}{(\omega + j2)^p} \tag{III.60}$$

for the 1-stage TIA, and

$$Z_t(\alpha \cdot \omega) = \frac{j4.8^p}{(\omega + j4.8)^p} \tag{III.61}$$

for the 3-stage TIA, both with the number of VA stages given by the variable p.

Table III.2: Rise time co-efficients.

Coefficient	Equation	Value
$X_{1,0}$	$\sqrt{(\frac{2.2\sqrt{2}}{2})^2}$	1.556
$X_{1,1}$	$\sqrt{(\frac{2.2\sqrt{2}}{2})^2 + (\frac{2.2}{2})^2}$	1.905
$X_{1,2}$	$\sqrt{(\frac{2.2\sqrt{2}}{2})^2 + 2(\frac{2.2}{2})^2}$	2.200
$X_{3,0}$	$\sqrt{(\frac{2.2\sqrt{2}}{2})^2}$	1.556
$X_{3,1}$	$\sqrt{(\frac{2.2\sqrt{2}}{2})^2 + (\frac{2.2}{4.8})^2}$	1.622
$X_{3,2}$	$\sqrt{(\frac{2.2\sqrt{2}}{2})^2 + 2(\frac{2.2}{4.8})^2}$	1.685

III.D.3 Bit Rate

The speed of the receiver amplifiers acting in cascade can be written in terms of the minimum signal rise time at the input to the decision circuit. This can be found by adding the square of the rise times of each amplifier and taking the square root of the sum:

$$t_{r,amps} = \sqrt{t_{r,TIA}^2 + p \cdot t_{r,VA}^2} \tag{III.62}$$

where p is the number of voltage amplifiers used in the receiver. Writing this in terms of α gives:

$$t_{r,amps} = \frac{X_{n,p}}{\alpha} \tag{III.63}$$

where X is given in Table III.2.

The rise time of the signal at the input to the digital buffer can be determined from the rise times of each of the receiver components – the amplifiers ($t_{r,amps}$), the decision circuit ($t_{r,DC}$), and the input signal rise time ($t_{r,in}$), as simply:

$$t_{r,out} = \sqrt{t_{r,in}^2 + t_{r,amps}^2 + t_{r,DC}^2} \tag{III.64}$$

The maximum bit-rate that can be supported with this rise time is written

$$BR_{max} = \frac{\zeta}{t_{r,out}} \tag{III.65}$$

where ζ determines what percentage of the bit period makes up the rise time. Larger values of ζ reduce the bandwidth requirement of the receiver, but increase the amount of intersymbol interference in the recovered signal at the input to the digital buffer. If the output rise time is approximated as a single pole response, then the bit-rate to 3-dB bandwidth ratio (a measure of the bandwidth efficiency) can be calculated to be

$$\frac{BR}{BW} = \zeta\frac{2\pi}{2.2} \tag{III.66}$$

In a synchronous NRZ receiver, ζ can be taken to be about 60% without significant signal degradation [24]. This corresponds to a bit rate to bandwidth ratio of approximately 1.7.

Receivers with a three-stage TIA are significantly slower than ones with a one-stage TIA, when both are constructed from identical amplifying stages. In general, it can be shown that when the number of stages in a feedback loop increases, the bandwidth decreases [61]. However, in order to determine when three-stage TIA based receivers are competitive, the transimpedance gain must be examined as well.

III.D.4 Transimpedance Gain

The overall transimpedance gain, TZ, is the receiver's output voltage divided by the input current, and is given by the voltage gain of the p-stage post-amplifier times the transimpedance of the TIA:

$$TZ = A_v^p Z_f \tag{III.67}$$

For a receiver to operate correctly, a minimum average optical input power is necessary. This is the optical power that results in a voltage swing ΔV to the decision circuit. Dividing ΔV by the transimpedance of the receiver, TZ, yields the required signal current.

$$i_s = \frac{\Delta V}{TZ} \tag{III.68}$$

Dividing i_s by the responsivity of the detector, R_{pd} (in *amps/watt*) yields the required average optical power:

$$\overline{P_o} = \frac{i_s}{2R_{pd}} \tag{III.69}$$

where the factor of two accounts for the assumption that half of the bits are on and half are off.

As mentioned in Section III.C.3, the value of ΔV for the decision circuits used here is $\frac{V_{dd}}{5}$. The required average optical power is then:

$$\overline{P_o} = \frac{V_{dd}}{10R_{pd}TZ} \tag{III.70}$$

Even though three-stage TIAs are generally slower than one-stage TIAs, they can provide higher sensitivities, indicating that they may be competitive at low bit rates. The optimization described below determines the break-even point between one and three-stage TIA based receivers.

III.D.5 Power

The electrical power dissipation of the (N+P)-stage receiver is determined from the gain stage bias current, I_b, and the power supply voltage, V_{dd}, and can be written:

$$P_d = [(N+P)I_b + I_{dc}]V_{dd} \tag{III.71}$$

where I_{dc} is the decision circuit bias current.

There is additional power dissipation due to the switching of the node capacitances in the receiver, but this component is orders of magnitude less than the power dissipation due to the bias current. This is because the signal swings and the capacitances involved are small.

III.D.6 Size

In the optimized receivers, the NMOS transistor M1 is always the largest transistor. This means the layout width of the gain stage cell is approximately

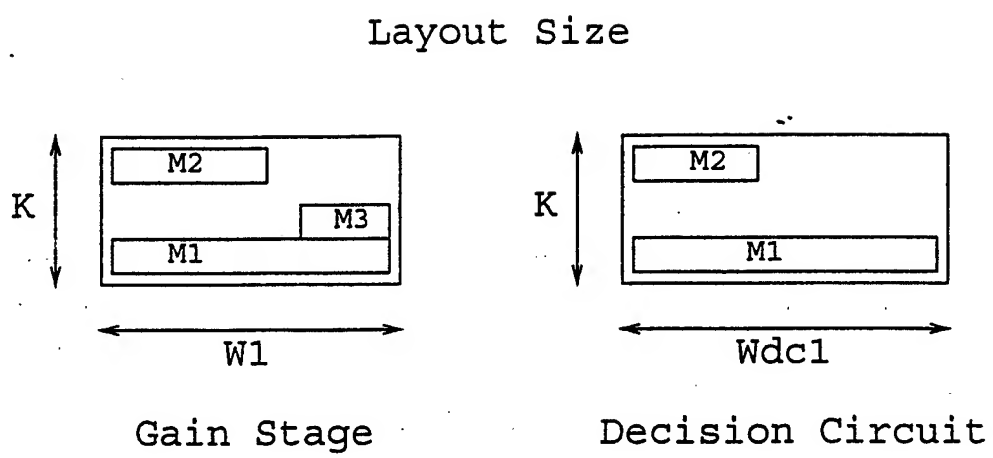


Figure III.21: Layout floorplan of receiver gain stage and decision circuit.

determined by the width of this transistor, W_1. The layout height of the gain stage cell is determined by the design rules of the technology. The design rules set the MOSFET source/drain diffusion lengths and the local interconnect widths. For a given technology, the layout height can be taken as a constant K. The total circuit area of a receiver with (N+P)-stages and a decision circuit with NMOS transistor width of W_{dc1} can then be approximated by

$$Area = (N + P)KW_1 + KW_{dc1} \tag{III.72}$$

This is shown in Figure III.21.

However, the physical circuit area may not be the limiting factor in determining the density of receivers. With the high power dissipation of these receivers, the thermal power density must be considered. In this case, with a maximum power density of P_{max} dictated by the cooling method, the effective size of the receiver is

$$Area = \frac{P_d}{P_{max}} \tag{III.73}$$

So, for example, a receiver that dissipates 1 mW of power on a chip that has a maximum power dissipation of 10 W/cm^2 requires 10,000 μm^2, or in other words, a pitch separation of 100 μm (assuming a square pixel).

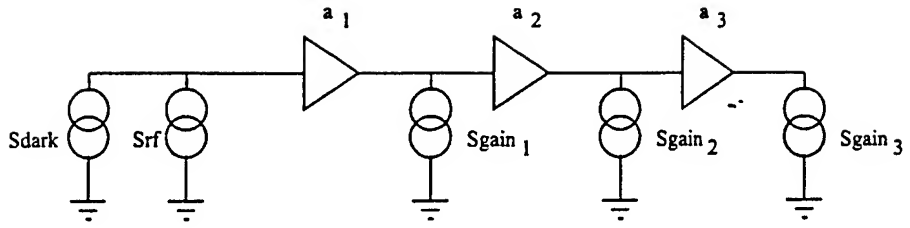


Figure III.22: Noise sources in the receiver.

III.D.7 Noise

The circuit noise introduced by the receiver and detector is referred to the receiver input for signal to noise ratio determination. Since the circuit noise usually dominates the optical signal shot-noise, it determines the maximum obtainable signal to noise ratio. The circuit noise consists of several components. The first component is the shot-noise of the leakage (dark) current of the detector. The second component is the thermal noise due to the feedback resistor. The third component is the thermal noise due to the gain-stage transistors. We examine each of these noise sources in turn. The noise sources are shown in Figure III.22.

The current noise spectral density of the shot noise due to the dark current of the detector is given by

$$S_{dark}(f) = 2qI_{dark} \tag{III.74}$$

where it is seen that this noise is white and acts at the input of the receiver.

The thermal noise due to the feedback resistor can be approximated as a current noise source at the input of the receiver with spectral density

$$S_{rf}(f) = \frac{4kT}{R_f} \tag{III.75}$$

where the approximation assumes that the forward current-gain through the amplifier is greater than that through the feedback resistor. [25] This assumption is easily met for any non-trivial design. This noise is also white.

The thermal noise in the gain stage itself is due to the channel resistance,

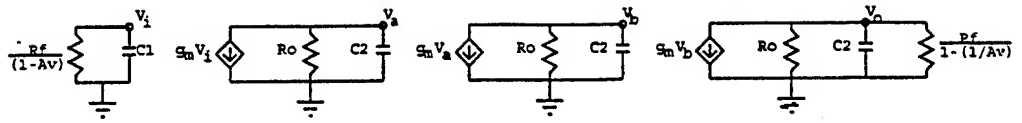


Figure III.23: TIA noise model.

and appears at the output of the gain stage as a noise current spectral density of

$$S_{gain}(f) = 4kT\Gamma\left(\sum g_m\right) \tag{III.76}$$

where $\sum g_m$ is shorthand for $g_{m1} + g_{m2} + g_{m3}$.

This noise can be referred to the input of the gain stage by dividing by the magnitude squared short-circuit current gain of the stage. Then, by dividing by the magnitude squared short-circuit current gains of all the preceding stages, the noise at any gain stage can be referred back to an input equivalent noise spectral density, as described by Moustakas in [25]. Thus, to complete the analysis, the short-circuit current gains must be determined. This will be done for the transimpedance amplifier and the voltage amplifier separately.

For the transimpedance amplifier, the non-feedback Miller equivalent amplifier may be analyzed, as shown in Figure III.23. The figure shows a three-stage TIA. The capacitance at the input to the first stage is

$$C_1 = C_{pd} + C_{in,amp} + C_{f,amp} \tag{III.77}$$

whereas the following gain stages have input capacitances of

$$C_2 = C_{out,amp} + C_{in,amp} + C_{f,amp} \tag{III.78}$$

The short-circuit current gain of each stage is found by shorting the output of that stage to ground, and solving for the current flowing through the short as a function of the current in the preceding stage. Since applying a short makes the voltage gain A_v of the circuit zero, the input referred feedback resistance $\frac{R_f}{1-A_v}$ and the output referred feedback resistance $\frac{R_f}{1-\frac{1}{A_v}}$ become simply R_f. The short circuit

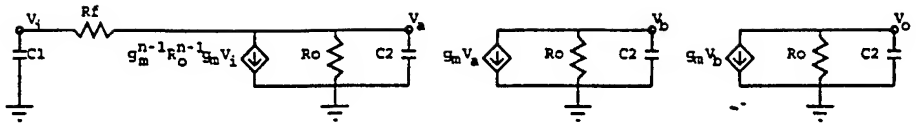


Figure III.24: VA noise model.

current gains can now be found:

$$a_1 = \frac{g_{m1}R_f}{1 + sR_fC_1} \tag{III.79}$$

$$a_2 = \frac{g_{m1}R_o}{1 + sR_oC_2} \tag{III.80}$$

where a_1 is the short-circuit current gain of the first stage, and a_2 is the short-circuit current gain of the following stages.

The model to determine the voltage amplifier current gains is shown in Figure III.24. The transimpedance amplifier is modeled by the first stage in this figure, where $n = 1$ for a one-stage TIA and $n = 3$ for a three-stage TIA. The short-circuit current gains are:

$$b_1 = \frac{g_{m1}^n R_o^{n-1} R_f}{1 + sR_fC_1} \tag{III.81}$$

$$b_2 = \frac{g_{m1}R_o(1 + sR_fC_1)}{g_{m1}^n R_o^n + 1 + s(R_f + R_o)C_1} \tag{III.82}$$

$$b_3 = \frac{g_{m1}R_o}{1 + sR_oC_2} \tag{III.83}$$

b_1 is the short-circuit current gain of the first (transimpedance) stage, b_2 is the short-circuit current gain of the first voltage amplifier stage, and b_3 is the short-circuit current gain of the following voltage amplifier stages.

The total input equivalent noise current spectral density can now be written

$$S_i(f) = S_{dark}(f) + S_{rf}(f) + S_{TIA}(f) + S_{VA}(f) \tag{III.84}$$

Where the noise due to the transimpedance amplifier is

$$S_{TIA}(f) = S_{gain}(f)\left(\frac{1}{|a_1|^2} + \frac{1}{|a_1|^2|a_2|^2} + \frac{1}{|a_1|^2|a_2|^2|a_2|^2}\right) \tag{III.85}$$

This equation is for a three-stage TIA - for a one stage TIA the last two terms in the equation are dropped.

The noise due to the voltage amplifier stages is

$$S_{VA}(f) = S_{gain}(f)\left(\frac{1}{|b_1|^2|b_2|^2} + \frac{1}{|b_1|^2|b_2|^2|b_3|^2}\right) \qquad \text{(III.86)}$$

This equation is for two voltage amplifier stages - for one stage, the last term in the equation is dropped. For no voltage amplifier stages, $S_{VA}(f) = 0$.

To reduce the complexity of the total noise equation, we keep only the dc terms and the terms with the input pole, $R_f C_1$. The higher order poles are ignored, because their effect is negligible after the integration over the receiver transfer function. We also assume that the feedback resistance is large enough so that $R_f \gg R_o$, and the gain $-g_{m1}R_o$ is written as A_v. The total input equivalent noise current spectral density can then be approximated:

$$S_i(f) = 2qI_{dark} + \frac{4kT}{R_f} + 4kT\Gamma\frac{\sum g_m}{g_{m1}^2}\left(\frac{1}{R_f^2}\left(\sum_{s=0}^{n-1} A_v^{-2s} + \sum_{s=0}^{p-1} A_v^{-2s}\right) + (2\pi f C_1)^2 \sum_{s=0}^{n+p-1} A_v^{-2s}\right) \qquad \text{(III.87)}$$

where $n+p$ is the number of gain stages in the receiver, n being the number of TIA stages and p being the number of VA stages. Note that this noise increases with frequency, thus it can be called "blue" noise.

The total noise equation demonstrates that at different frequencies, the noise of the voltage amplifier is treated differently. At high frequencies, where the term $(2\pi f C_1)^2$ dominates, the noise from the voltage amplifier is divided down by the voltage gain of the transimpedance amplifier stages - hence the high frequency noise from the voltage amplifier does not greatly contribute to the total noise. However, at low frequencies, where the term $\frac{1}{R_f^2}$ dominates, the noise from the voltage amplifier is not divided by the gain of the transimpedance amplifier stages. The low frequency noise of the first stage of the voltage amplifier has just as much effect on the total noise as the low frequency noise of the first stage of the transimpedance amplifier. This difference between high and low frequency noise is due to the changing impedance of the input capacitance C_1. At high frequencies,

the low impedance of C_1 means most of the input current flows through C_1 instead of R_f. Thus, the effect of the feedback is reduced and the transimpedance amplifier acts more like a cascaded series of gain stages.

When integrating over frequency, the dominant component of the total noise equation is the high frequency term. This means the noise of the voltage amplifier is a minor contributor to the total noise, as it is effectively divided by the gain of the transimpedance amplifier stages. However, the difference between low frequency and high frequency noise is important in the determination of the supply rejection and the effects of parameter variations, as will be shown in the next section.

The input equivalent current noise is found by integrating over frequency the total input equivalent noise current spectral density multiplied by the squared normalized receiver transfer function.

$$\left\langle {i_c}^2 \right\rangle = \int_0^\infty S_i(f) \frac{|Z_T(f)|^2}{|Z_T(0)|^2} df \tag{III.88}$$

This can be written

$$\left\langle {i_c}^2 \right\rangle = \left[2qI_{dark} + \frac{4kT}{R_f} + \frac{4kT\Gamma \sum g_m}{(g_{m1}R_f)^2} \left(\sum_{s=0}^{n-1} A_v^{-2s} + \sum_{s=0}^{p-1} A_v^{-2s} \right) \right] \frac{J_{n,p}}{t_{r,amps}} + \left[4kT\Gamma \frac{\sum g_m}{g_{m1}^2} (2\pi C_1)^2 \sum_{s=0}^{n+p-1} A_v^{-2s} \right] \frac{K_{n,p}}{t_{r,amps}^3} \tag{III.89}$$

The values of $J_{n,p}$ and $K_{n,p}$ depend on the transfer function of the receiver, $Z_T(f)$, and are given by

$$J_{n,p} = X_{n,p} \int_0^\infty \frac{|Z_T(\alpha f)|^2}{|Z_T(0)|^2} df \tag{III.90}$$

$$K_{n,p} = X_{n,p}^3 \int_0^\infty f^2 \frac{|Z_T(\alpha f)|^2}{|Z_T(0)|^2} df \tag{III.91}$$

Since the transfer functions are known, the values of the integrals in (III.90) and (III.91) can be determined for each receiver configuration. The calculated values are given in Table III.3. The receiver configuration is coded as N+P,

Table III.3: Calculated noise coefficients for different receiver configurations.

Receiver Configuration	$J_{n,p}$	$K_{n,p}$
(1+0)	0.389	0.0477
(1+1)	0.381	0.0350
(1+2)	0.374	0.0322
(3+0)	0.367	0.0309
(3+1)	0.363	0.0287
(3+2)	0.362	0.0274

where N is the number of stages in the transimpedance amplifier, and P is the number of stages in the voltage amplifier.

The two integrands in (III.90) and (III.91) are graphed versus frequency in Figure III.25 for single-stage TIA receivers (N=1), and in Figure III.26 for three-stage TIA receivers (N=3). The graphs indicate that the dominant noise sources at frequencies below $\omega = \alpha$ are from the photodiode dark current and the thermal noise of the feedback resistor. The dominant noise source at frequencies above $\omega = \alpha$ is from the gain-stage transistors. Depending on the relative sizes of the two terms, there can exist a peaking in the noise spectra at $\omega = \alpha$. This peaking exists when the gain-stage open-loop bandwidth is much larger than the signal bandwidth. [62] However, the optimized receiver designs presented here do not exhibit this peaking, as the design criteria for MFM response ensures that the gain-stage bandwidth is not much larger than the signal bandwidth. The input equivalent noise power spectra is shown in Figure III.27 for two typical receivers, demonstrating the lack of noise peaking.

Note that $J_{n,p}$ and $K_{n,p}$ serve a similar function as the constants I_2 and I_3 as introduced by Smith and Personick in [26]. However, I_2 and I_3 are given in terms of a bit rate, whereas the constants introduced here are in terms of the intrinsic rise time of the receiver amplifiers. Using the intrinsic rise time eliminates the common error of using the operating bit rate as the bit rate in the Smith and Personick noise calculations. Incorrect usage of the bit rate is discussed extensively

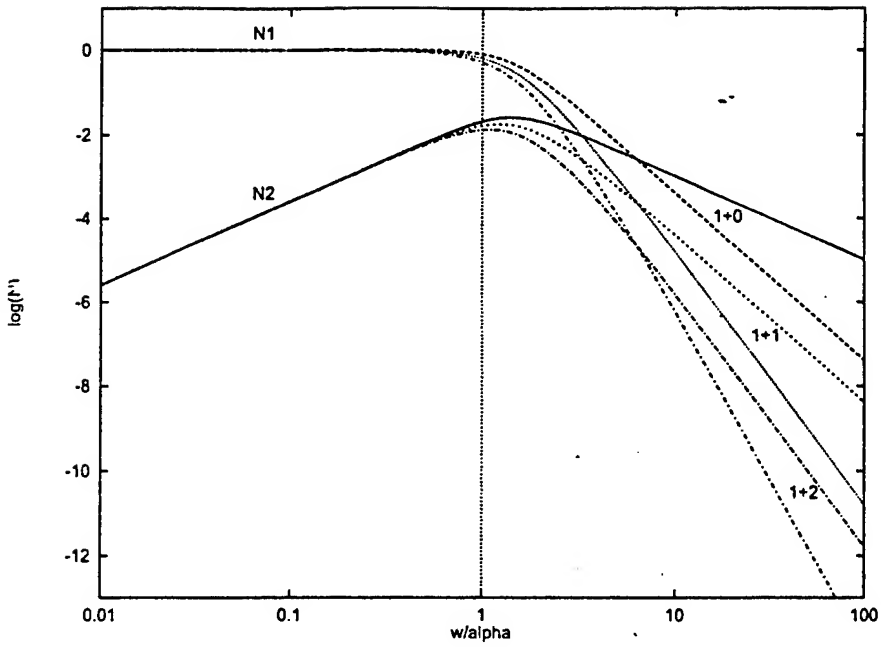


Figure III.25: Graph of $N1 = \frac{|Z_T(f)|^2}{|Z_T(0)|^2}$ and $N2 = f^2\frac{|Z_T(f)|^2}{|Z_T(0)|^2}$ for single-stage transimpedance amplifier receivers (N=1).

in [23].

Finally, there are several additional sources of noise that are omitted in this analysis. The $1/f$ noise in the gain transistors can be a significant effect at low frequencies, but becomes negligible when the integration is performed over the receiver bandwidth to obtain the total noise power. Likewise, the shot noise due to the Poisson arrival rate of the photons is typically at least an order of magnitude smaller than the circuit noise. A complete analysis of this signal dependent noise can be found in [23], where it is shown to be a minor contributor to the total noise of the receiver.

III.D.8 Bit Error Rate

The signal to noise ratio of the receiver can now be determined. To do this, the input equivalent noise power is determined by referring all of the noise

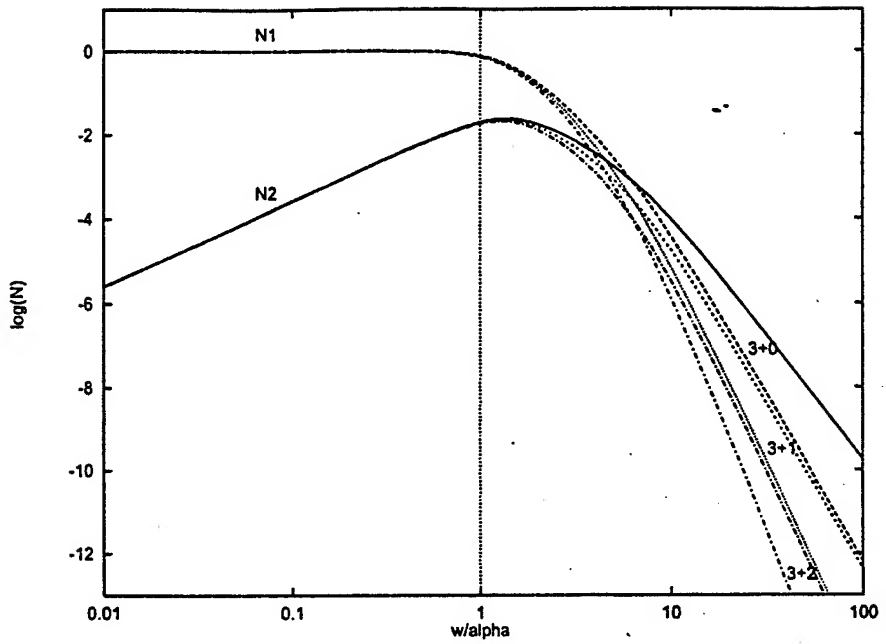


Figure III.26: Graph of $N1 = \frac{|Z_T(f)|^2}{|Z_T(0)|^2}$ and $N2 = f^2\frac{|Z_T(f)|^2}{|Z_T(0)|^2}$ for 3-stage transimpedance amplifier receivers (N=3).

sources to the input of the receiver. The noise power is written, following III.69, as:

$$P_n = \frac{\sqrt{\langle i_c^2 \rangle}}{2R_{pd}} \tag{III.92}$$

The signal to noise ratio is written Q, and is

$$Q = \frac{\overline{P_o}}{P_n} \tag{III.93}$$

where P_o is given by III.69.

This ratio determines the intrinsic noise limited bit error rate of the link. A hypothetical distribution of received values for a transmitted 1 and a transmitted 0 are shown in figure III.28. A threshold is established where if the received value is below the threshold, a 0 is output, and if it is above the threshold, a 1 is output. Assuming the noise is Gaussian, the probability of making an error is simply the integral of the distribution that lies on the other side of the threshold (the shaded

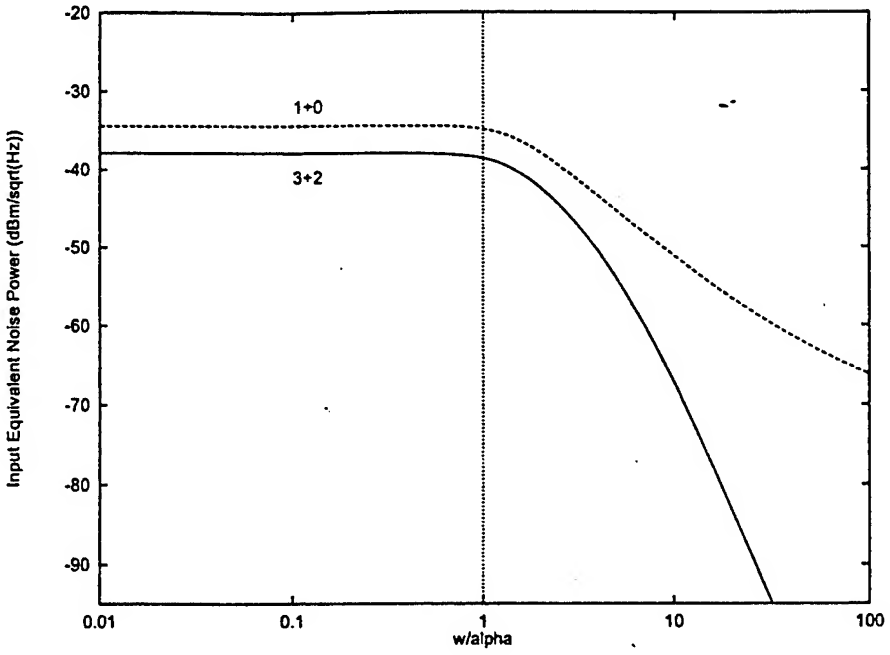


Figure III.27: Graph of input equivalent noise power versus frequency for two typical optimized receivers in a 0.35 μm process.

area in the figure).

Thus, the probability of error when a 1 is transmitted is

$$P(e|1) = \frac{1}{2} erfc\left[\frac{(S_1 - S_t)}{\sqrt{2}\sigma_1}\right] \tag{III.94}$$

and the probability of error when a 0 is transmitted is

$$P(e|0) = \frac{1}{2} erfc\left[\frac{S_t}{\sqrt{2}\sigma_0}\right] \tag{III.95}$$

The average probability of error is the weighted average of these two error probabilities, the weightings being determined by the probability of actually transmitting a 1 or a 0:

$$P(e) = P(1)P(e|1) + P(0)P(e|0) \tag{III.96}$$

In the special case where a 1 or 0 bit is equally probable, and the noise power of $P_n = 2\sigma$ is the same for both the 1 and 0 bits, $S_t = \frac{S_1}{2}$ and the BER is

$$BER = \frac{1}{2} erfc\left[\frac{S_1}{2\sqrt{2}\sigma}\right] = \frac{1}{2} erfc\left[\frac{Q}{\sqrt{2}}\right] \tag{III.97}$$

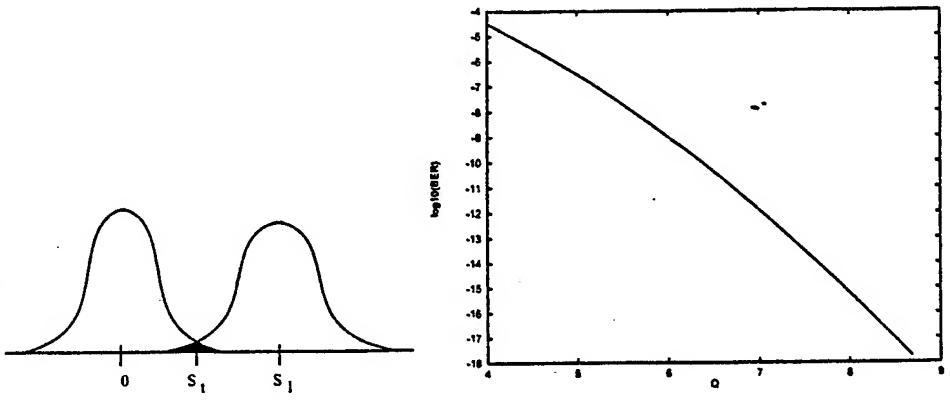


Figure III.28: Probability distribution and bit-error rate as a function of Q.

This is graphed as a function of Q, the signal to noise ratio, in Figure III.28.

Thus, to obtain a bit-error rate of 10^{-12} requires a signal to noise ratio of approximately $Q = 7$. The conventional analysis would stop here, and determine the receiver sensitivity based on this required signal to noise ratio. This would be appropriate for a single long-range, error corrected link with precisely tuned and electrically isolated receiver components. In particular, it assumes that a perfect decision circuit exists at the output of the receiver to perform the thresholding operation.

The high-density, short range, un-coded links proposed here are in a quite different electrical environment. They share a silicon IC with high-speed processing circuitry, and as such are subjected to power supply fluctuations. They are fabbed in a digital CMOS process, with parameters that vary from lot to lot and from device to device. The decision circuit cannot be ignored in the analysis, for its output must conform to the signaling requirements of VLSI circuits. This signaling requirement sets a noise margin, which the output of the decision circuit must meet. Thus, the optical power requirement stated in Equation III.69 is based on the noise margin required at the output of the decision circuit, and not the circuit noise of the receiver. However, the conventional noise analysis is useful in that it sets a floor for the sensitivity of the receiver.

III.D.9 Power supply rejection and de-coupling

To understand how the receiver will respond to power supply fluctuations in a mixed-signal IC, this section examines the power supply rejection ratio (PSRR) of the receiver gain stage. The PSRR is a measure of the sensitivity of the gain stage to power supply noise. The mixed-signal chip environment has many potential sources of power supply noise. High speed digital logic, fast rise-time I/O circuits, and the receiver itself contribute, through interaction with the supply line impedance, to power supply fluctuations. Power supply noise reduces the noise margin of the receiver and can cause bit errors. Even worse, switching noise generated by the receiver can induce self-oscillation, with the positive feedback path being the supply rails.

Board level design techniques are used to reduce the effect of power supply noise. Some standard techniques are the use of short, fat supply busses, multiple vias, split power planes, and star connections. [63] Analysis of signal return currents is also required to avoid large current loops. Decoupling capacitors are used to provide low impedance paths for high-frequency noise on the supply lines. However, the combination of the decoupling capacitance and the inductance in the supply lines leads to a resonance frequency which, if located near the operating frequency of the board, can significantly increase the supply noise. Careful choice of the decoupling capacitors is necessary to avoid making the noise situation worse. [62] Decoupling capacitors can also be included at the chip level. While limited in total capacitance, these capacitors have a low series inductance and are good for suppressing noise at very high frequencies.

The PSRR is defined as

$$PSRR = \frac{A}{A_p} \tag{III.98}$$

where A is the signal gain and A_p is the gain from the power-supply; that is, a disturbance of v on the supply appears as $A_p v$ at the gain stage output. [64] The small signal model for the analysis of A_p is shown in Figure III.30. The capacitors

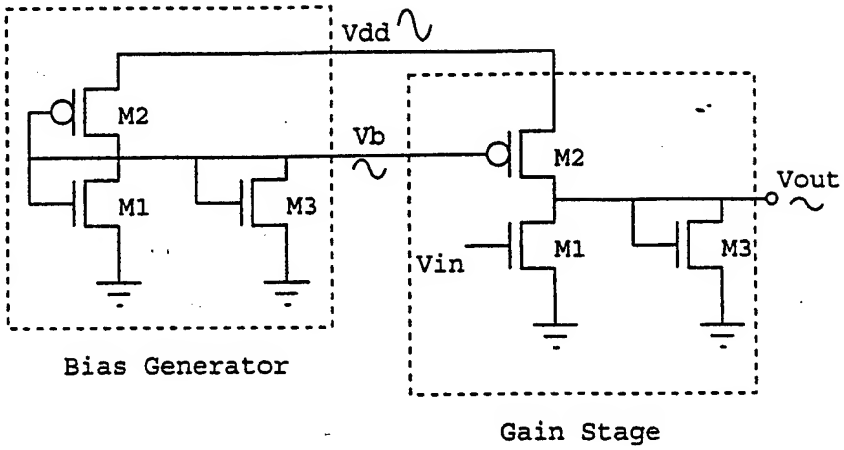


Figure III.29: Power supply noise on critical nodes.

C_{b1} and C_{b2} are the decoupling capacitors. Note that C_{b1} is the traditional supply bypass capacitor, and that C_{b2} is an additional bypass from v_{dd} to V_b. The rationale for this additional bypass capacitor is explained below. C_{v2} is the overlap capacitance of the bias transistor (M2) gate to the gain stage output node. R_{b2} and R_{b3} are the small-signal resistances of the PMOS and NMOS transistors in the bias generator, respectively. Solving for v_{out} in terms of v_{dd} yields:

$$v_{out} = v_{dd}\frac{(g_{m2} - sC_{v2})R_{b2} + (g_{d2} + sC_{v2})(R_{b2} + R_{b3} + sC_{b2}R_{b2}R_{b3})}{(g_{d1} + g_{d2} + s(C_o + C_{v2}))(R_{b2} + R_{b3} + sC_{b2}R_{b2}R_{b3})} \tag{III.99}$$

Making use of the following simplifications:

$$g_d + g_{d2} \approx g_d \tag{III.100}$$

$$C_o + C_{v2} \approx C_o \tag{III.101}$$

$$R_{b2} + R_{b3} \approx R_{b2} \tag{III.102}$$

$$g_{m2} + g_{d2} \approx g_{m2} \tag{III.103}$$

gives us an equation for A_p.

$$A_p = \frac{s^2C_{v2} + sg_{d2} + \frac{g_{m2}}{C_{b2}R_{b3}}}{(sC_o + g_d)(s + \frac{1}{C_{b2}R_{b3}})} \tag{III.104}$$

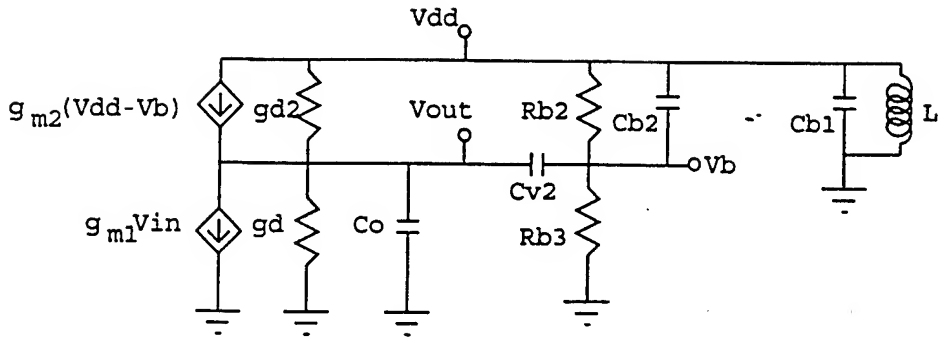


Figure III.30: Small signal circuit for power supply rejection analysis.

The gain stage has a signal gain described by

$$A = \frac{g_{m1}}{sC_o + g_d} \tag{III.105}$$

The PSRR can then be written

$$PSRR = \frac{g_{m1}(s + \frac{1}{C_{b2}R_{b3}})}{s^2C_{v2} + sg_{d2} + \frac{g_{m2}}{C_{b2}R_{b3}}} \tag{III.106}$$

At dc, the PSRR is the ratio of g_{m1} to g_{m2}. The numerator of Equation III.106 adds a zero at $\frac{-1}{C_{b2}R_{b3}}$. The denominator adds a pair of poles with real part $\frac{-g_{d2}}{2C_{v2}}$.

The rationale for bypass capacitor C_{b2} can now be explained - the additional zero can be used to boost the PSRR, especially around the operating frequency of the receiver and the resonance frequency of the supply decoupling circuit, where the worst noise is expected. C_{b2} works by lowering the impedance between v_{dd} and V_b, thus keeping the gate-source voltage approximately constant on transistor M2. This maintains the current bias of M1, thus reducing the effect of the supply noise on the output of the gain stage.

With this analysis of the PSRR of the gain stage, the sensitivity of the complete receiver to the power supply noise can be developed. We will follow the procedure used to calculate the equivalent input noise current in the previous section, i.e. at each stage, the current due to the supply noise will be referred back

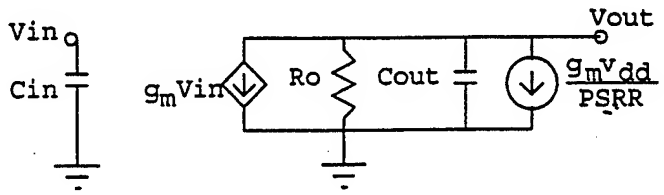


Figure III.31: Model of supply noise in the gain stage.

to the input of the receiver. Note that unlike in the noise case, here the current sources at each stage are correlated, since they are derived from the same supply signal. Again, we will use the circuit models shown in Figure III.23 and Figure III.24.

The current source which represents the supply's effect on the gain stage output can be written

$$i_s(f) = \frac{g_{m1} v_{dd}}{PSRR(f)} \tag{III.107}$$

as shown in Figure III.31. Using the short-circuit current gains described above, the equivalent input current can be written:

$$i_{eq}(f) = \frac{Z_T(f) v_{dd}}{Z_T(0) PSRR(f)} \left(\frac{1}{R_f} \left[\sum_{s=0}^{n-1} \frac{1}{A_v^s} - \sum_{s=n}^{n+p-1} \frac{A_v^n + 1}{A_v^s} \right] + j2\pi C_1 \left[\sum_{s=0}^{n-1} \frac{1}{A_v^s} - \sum_{s=n}^{n+p-1} \frac{1}{A_v^s} \right] \right) \tag{III.108}$$

Note that the gain A_v is negative, so that unlike the total noise equation where the gain term is squared, the terms in the sums in III.108 alternate in sign. In fact, assuming identical gain stages, the effect of the power supply noise on a three-stage TIA receiver is less than that of a one-stage TIA receiver. This is because at each gain stage, the supply noise is out of phase with the amplified supply noise of the previous stage, effectively canceling out part of the noise from that stage. Of course, the optimized gain stage design is different for one-stage and three-stage TIA receivers due to the different stability requirements of both types of receivers.

To demonstrate the accuracy of the model, Figure III.32 shows the results of calculating the magnitude of equation III.108 and HSPICE simulation results for

an optimized 3+2 receiver in a 0.35 μm technology. The graph shows the amount of supply noise that produces a voltage at the input to the decision circuit equivalent to that produced by the receiver's required input current - in other words, a signal to noise ratio of one. The model agrees well with the simulation results within the frequencies of interest. A roll off is seen in the HSPICE simulation data at higher frequencies, but this is at voltage levels significantly above the minimums around the receiver's operating frequency, where the worst supply noise would be.

Two different values of the bias decoupling capacitance C_{b2} are graphed. The benefits of a larger value of C_{b2} are clearly seen, as a four times improvement in immunity to supply noise at the operating frequency is gained by raising C_{b2} from $2pF$ to $20pF$. To determine the total noise due to the supply, equation III.108 must be integrated over all frequencies. This means that the frequency spectrum of the supply noise must be known.

Assuming most of the supply noise is at the receiver operating frequency, to achieve a signal to supply noise ratio of 10 requires that the supply noise be less than $7mV$ for $C_{b2} = 2pF$, and less than $33mV$ for $C_{b2} = 20pF$, for the example receiver analyzed in Figure III.32. Whether this level of noise can be achieved depends on the implementation details, but at least the later case should be practical with careful attention to die and board layout. The decoupling capacitor increases the circuit area required for the bias generator, but this overhead can be reduced if one bias generator is used for multiple receivers.

This particular receiver example is of one of the most sensitive receiver configurations to supply noise. A comparison of the decoupling requirements for different optimized receiver configurations in 0.35 μm CMOS is shown in Figure III.33. This graph shows the decoupling capacitance required to provide a SNR of 10 in the presence of 25 mV of noise on V_{dd} at the receiver operating frequency. A minimum decoupling capacitance value of 250 fF is assumed. The numbers next to each point describe the configuration of the receiver, N+P, where N is the number of stages in the TIA and P is the number of stage in the VA. The receivers

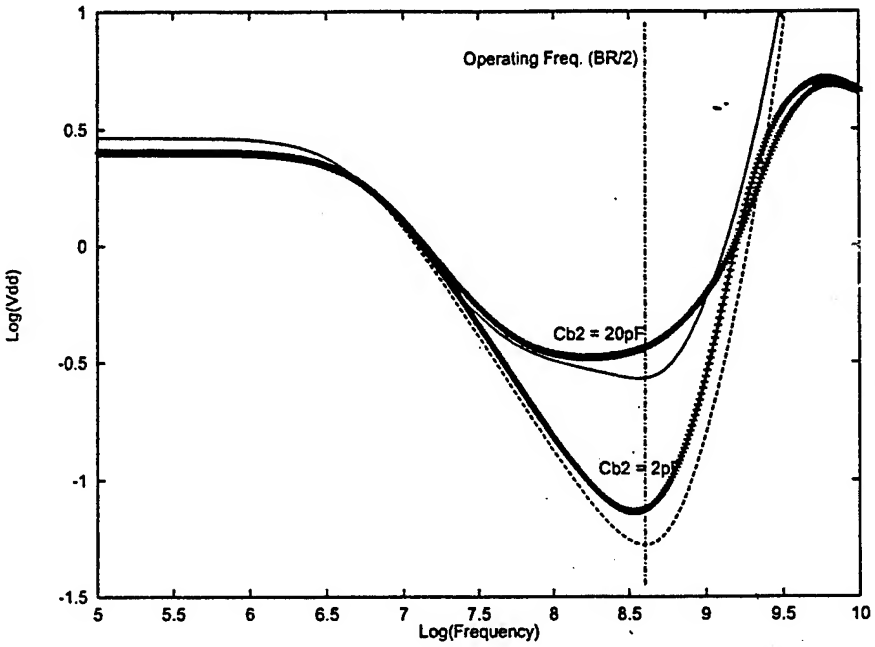


Figure III.32: Model (solid lines) and HSPICE simulation (crosses) of the amount of supply noise at different frequencies that produces a signal to noise ratio of one, for an optimized 3+2 receiver in a 0.35 μm process.

which have been optimized for minimum optical power are shown by diamonds, and the receivers optimized for minimum total power (with $\eta = 50$) are shown by crosses. The receiver optimization procedure is described in detail in Section III.E.3.

This graph demonstrates that the receivers with fewer stages require smaller decoupling capacitances. Since these receiver are less sensitive to start with, it follows that they are also less sensitive to supply noise. As the receivers with fewer stages are only optimum at higher bit-rates, the decoupling requirement decreases with increasing bit-rate. Also, the total power optimized receivers require less decoupling. This is because they have traded sensitivity for power efficiency, and are thus less sensitive to supply noise. Finally, the requirement for more than 10 pF of decoupling for the slowest optical power optimized receivers

would be expensive to implement on-chip. The other decoupling values, which are less than 4 pF, could be implemented on-chip with little overhead.

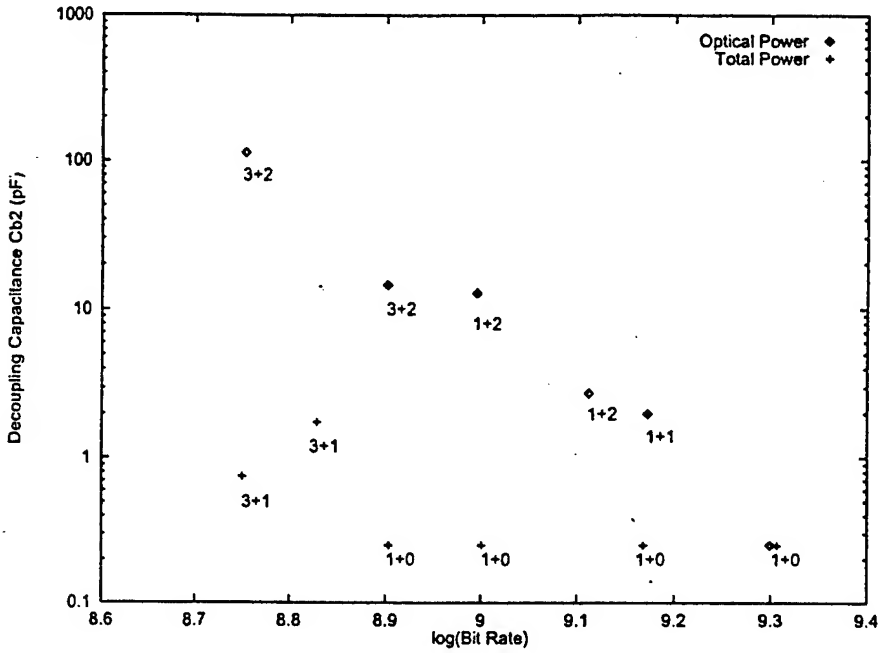


Figure III.33: Decoupling capacitance C_{b2} necessary for SNR=10 with 25 mV of noise on V_{dd}, for receivers optimized for optical power and total power in 0.35 μm CMOS.

III.D.10 Parameter variations

There are two aspects of parameter variations in CMOS processing which affect the operation of FSOI receivers. These two types of parameter variations are described in Section II.A.3 and are summarized here. This section then presents an analysis of their effect on FSOI receiver performance.

The first type of parameter variation is the "lot-to-lot" variation, where all of the transistors on a wafer or within a run have parameters which vary from the standard or nominal parameters. The second type of parameter variation is transistor mismatch within a single circuit. This mismatch is a smaller relative

shift in transistor parameters than the "lot-to-lot" variations. However, because this variation affects different transistors differently within the same circuit, it can cause offsets between the operating points of identical stages. The receivers described here use dc-coupled cascaded gain stages. Thus it is especially important to keep these offsets small, as an offset in the first stage is amplified by following stages.

Lot-to-Lot variations

As mentioned in Section II.A.3, the "lot-to-lot" variations in a process are taken into account by providing process corner models. These corner models predict the performance of the NMOS and PMOS devices at the extremes of the process variations.

To model the effect of process variations on the optimized receivers presented in this analysis, the receiver characteristics are calculated for the MOSFET model parameters from the four process corners: fast, slow, up, and down. This is not a design optimization, as the receiver designs have already been optimized with the nominal process models, and their design parameters are fixed. The only parameter that can be changed is the feedback resistance — it can be modified through the use of the tunable voltages at the gate of the feedback transistors, V_{nfb} and V_{pfb}. Using the fixed receiver transistor sizes and number of amplifiers, the analysis program finds a new feedback resistor value that produces the required MFM response for the new MOSFET parameters. The receiver speed and sensitivity can then be determined.

The performance in terms of optical sensitivity versus bit-rate is shown in Figure III.34 for six receivers in 0.35 μm CMOS, optimized for minimum optical power. The receiver configuration (N+P) is shown in the figure for each receiver. The results of the nominal optimization are shown by the dashed line. Around each nominal point are four other points, which give the performance of that receiver for the four process corners. It can be seen that the "fast" corner increases the

speed of each receiver, but requires somewhat more optical power. The same is true to a smaller extent for the "down" corner. Likewise, the "up" corner and the "slow" corner increasingly slow down the receiver, while reducing the optical power requirement. It is interesting to note that the process variations affect the bit-rate much more than the optical power requirement, in contrast to the large change in optical power requirement obtained through the optimization of the transistor sizes and number of stages.

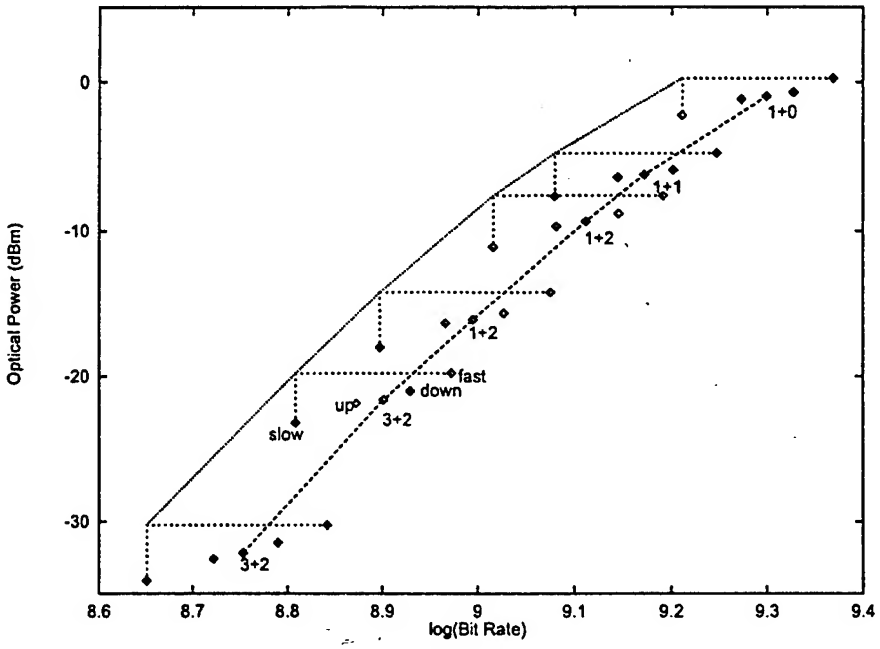


Figure III.34: Plot of optical power requirement versus bit-rate, showing performance at all four process corners, for receivers optimized for optical power in 0.35 μm CMOS. Worst case optical power and bit-rate combination is also graphed.

Figure III.35 shows the same corner analysis for six 0.35 μm receivers optimized for total power, with $\eta = 50$, as described in the next section. The general trend of the four corners is the same, with the "fast" corner producing the highest speed, lowest sensitivity receivers, and the "slow" corner vice-versa. The optical sensitivities of these receivers, however, are found to be less dependent on

process variations than the receivers optimized for minimum optical power.

The worst case performance of the receiver is found by using the speed of the "slow" receiver with the optical power requirement of the "fast" receiver. This is shown by the dotted line in the figures. The result is a shift upwards in the optimized curve by about $+7\ dBm$ in optical power requirement for the receivers optimized for minimum optical power, and by $+4\ dBm$ for the receivers optimized for minimum total power. In addition, the switching point between different receiver configurations moves downward in bit-rate.

The remainder of this analysis presents the results from the nominal process models. To determine the worst-case performance over "lot-to-lot" process variations, the shift in the curve described above can be applied.

Finally, to generate the on-chip voltages V_{nfb} and V_{pfb} which track the "lot-to-lot" process to properly tune the feedback resistance is an area for further research.

Transistor mismatch

Using the mismatch equations for the threshold voltage V_t and current factor β developed in Section II.A.3, together with the square-law I-V relationship of the MOS transistor given in Equation II.1, the variance in the bias current of two identical transistors with identical biasing can be written:

$$\sigma^2(i) = \frac{A_\beta^2 I^2 + A_{VT}^2 g_m^2}{W \cdot L} \tag{III.109}$$

Applying this formula to the three transistors in the receiver gain stage, and adding the square of the current variances gives

$$\sigma^2(i) = \frac{1}{L_{min}} \left[I_b^2 \left(\frac{A_{\beta n}^2}{W_1 + W_3} + \frac{A_{\beta p}^2}{W_2} \right) + \left(\frac{A_{VTn}^2 (W_1 + W_3) g_{m1}^2}{W_1^2} + \frac{A_{VTp}^2 g_{m2}^2}{W_2} \right) \right] \tag{III.110}$$

Where I_b is the gain stage bias current flowing through transistor M_2. Following the analysis for the input equivalent noise given in Section III.D.7, and

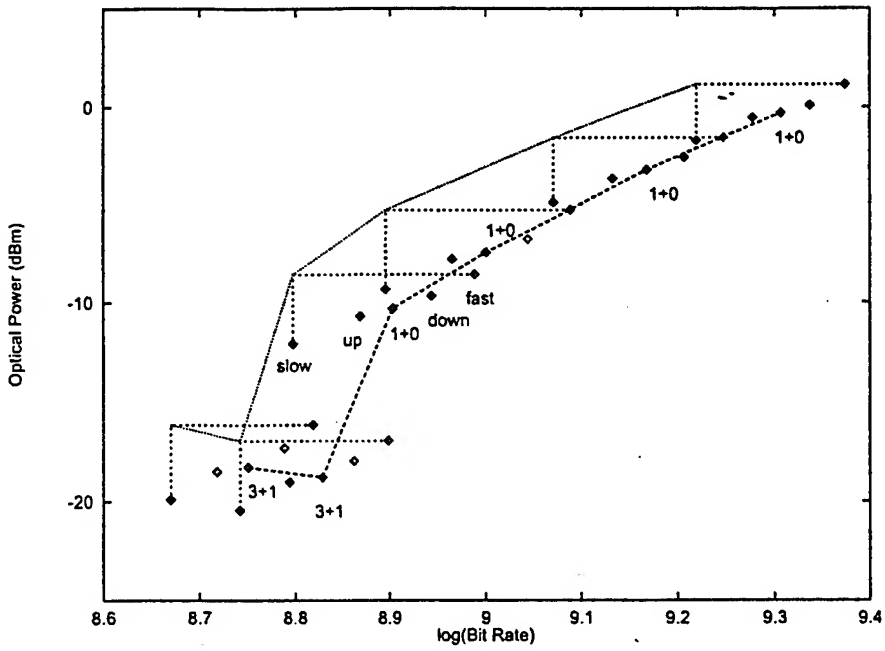


Figure III.35: Plot of optical power requirement versus bit-rate, showing performance at all four process corners, for receivers optimized for total power ($\eta = 50$) in 0.35 μm CMOS. Worst case optical power and bit-rate combination is also graphed.

noting that this noise source is at $f = 0$ (DC), the input equivalent current due to parameter variations can be written:

$$\left\langle {i_c}^2 \right\rangle = \frac{\sigma^2(i)}{\left(g_{m1} R_f\right)^2} \left(\sum_{s=0}^{n-1} A_v^{-2s} + \sum_{s=0}^{p-1} A_v^{-2s} \right) \qquad \text{(III.111)}$$

This current is essentially a variable DC offset which is added to the signal current. If it is small enough, it can be included as a noise source in the signal to noise ratio. It is possible to calibrate out this offset, using the current bias shown in Figure III.2. However, this would require an auto-zero or calibration operation and the ability to locally store the calibrated current value for each receiver. For example, this type of auto-zero operation is popular in flash ADCs, where each comparator is calibrated during part of the conversion cycle. It is best implemented

when the gain stages are AC coupled and the signal is a RZ (return-to-zero) format, so that the calibration can be performed during the zero period of each data bit. The receivers analyzed here are DC coupled, so that no signal coding is required, and use NRZ (non-return-to-zero) data format for highest speed. Thus calibration is more difficult for these receivers, and is an area for continued research.

Note that if the offset is too large, the amplifiers in the receiver will saturate. In this case, there is no way to properly tune the current bias, because there is no current bias value where all of the amplifiers will be out of saturation and in the high-gain region. When this happens, the small signal analysis given previously is no longer valid, and the receiver characteristics will suffer in terms of speed, jitter, and sensitivity. In fact, this has led other researchers to conclude that optical receivers will require complicated synchronization circuitry to compensate for the jitter induced by parameter variations. [65] However, that paper assumed a receiver with many stages, with no justification for the number of stages used. The optimization used in this analysis finds that, for high speed receivers, the number of stages is much smaller than that used in [65].

To see if the offset is too large, the signal to offset ratio can be found. Figure III.36 plots the calculated signal to offset ratios for 0.35 μm receivers optimized for optical power and total power. The worst signal to offset ratio is about 10 for the most sensitive receiver. This level of offset will not saturate the receiver stages and can be compensated by increasing the optical power by 10 %. The less sensitive receivers all have better signal to offset performance, indicating that the transistor mismatch offset is not a serious problem for these receivers.

III.E Optimization and Comparison

III.E.1 Approximate analysis

Consider the receiver with n TIA stages and p VA stages. Summarizing the above equations, the speed of the receiver amplifiers is determined by their

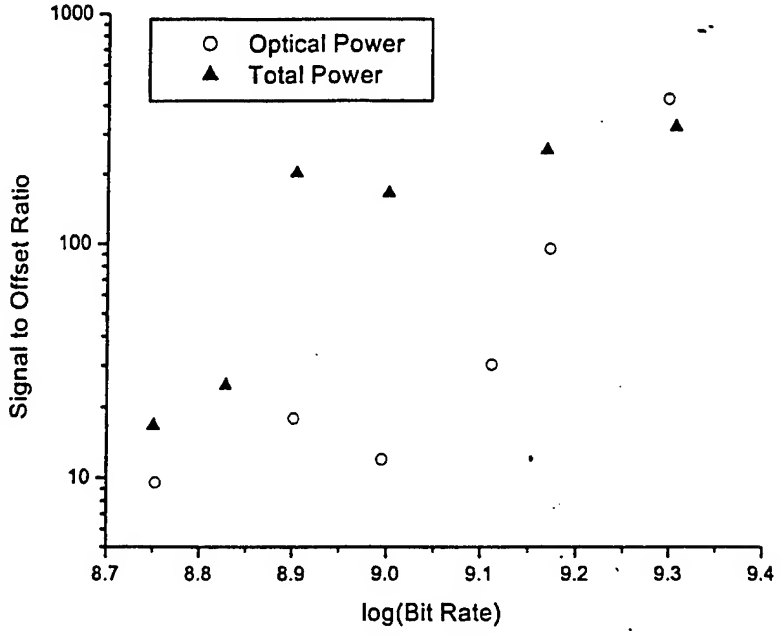


Figure III.36: Signal to offset ratio for receivers optimized for optical power and total power in 0.35 μm CMOS.

risetime, $t_{r,amps} = \frac{X_{n,p}}{\alpha}$. The sensitivity of the receiver amplifiers is given by $TZ = A_v^p Z_f$, which is the transimpedance gain of the TIA times the gain of the voltage amplifier.

As a simplified analysis, assume that the gain stage provides a constant gain-bandwidth product, $A_v p_{out} = \frac{g_m}{C_{out}} = GBW$. Thus, $p_{out} = \frac{GBW}{A_v}$. For the 1-stage TIA, this means

$$\alpha = \frac{GBW}{b \cdot A_v} \tag{III.112}$$

where $b = 2$ for the 1-stage TIA, and $b = 4.8$ for the 3-stage TIA.

Thus, the gain can be written in terms of the maximum bit-rate (i.e. the bit-rate assuming $t_{r,in} = 0$ and $t_{r,DC} = 0$):

$$A_v = \frac{\zeta \cdot GBW}{b \cdot X_{n,p} \cdot BR} \tag{III.113}$$

The transimpedance gain value can be approximated:

$$Z_f = Rf = \frac{a \cdot A_v^{n+1}}{GBW \cdot C_{in}} \qquad \text{(III.114)}$$

where $a = 2$ for the 1-stage TIA and $a = 6$ for the 3-stage TIA.

Finally, using the above equations, we can write the transimpedance in terms of the bit-rate as:

$$TZ = \frac{a \cdot GBW^{n+p}}{Cin} \left(\frac{\zeta}{b \cdot X_{n,p} \cdot BR} \right)^{n+p+1} \qquad \text{(III.115)}$$

The optimum receiver is the one which maximizes equation III.115 at a given bit-rate. If we assume the input capacitance is dominated by the photodiode capacitance, then the term C_{in} will be the same for all the receiver amplifier combinations. The bit-rate at which the optimum receiver switches between different receiver configurations can be found by solving equation III.115 for the bit-rate that makes the transimpedance the same for the different values of n and p. The result is shown in figure III.37. The optimum receiver switches between the 1+0 receiver to the 1+1 receiver at:

$$BR = \frac{\zeta X_{1,0}^2}{2X_{1,1}^3} \cdot GBW = 0.105 \cdot GBW \qquad \text{(III.116)}$$

Then it switches between the 1+1 and 1+2 receiver at:

$$BR = \frac{\zeta X_{1,1}^3}{2X_{1,2}^4} \cdot GBW = 0.089 \cdot GBW \qquad \text{(III.117)}$$

Finally, it switches between the 1+2 and 3+2 receiver at:

$$BR = \frac{4\sqrt{3}\zeta X_{1,2}^2}{4.8^3 X_{3,2}^3} \cdot GBW = 0.038 \cdot GBW \qquad \text{(III.118)}$$

The 3+0 and 3+1 receivers do not provide the maximum transimpedance at any bit-rate.

Of course, this analysis is very approximate, but the form of figure III.37 is reproduced by the numerical simulation described below. However, this simplified analysis cannot take into account the total power dissipation optimization, which must be determined numerically.

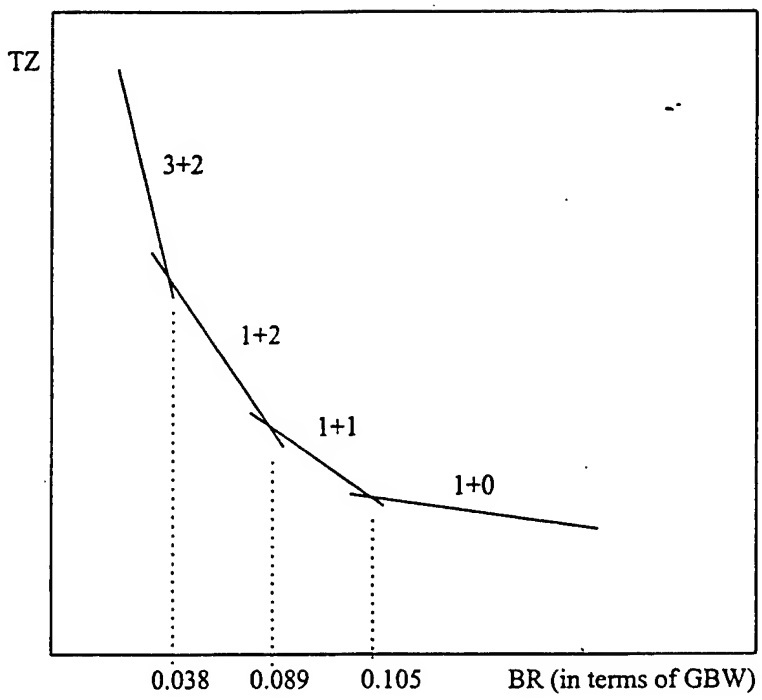


Figure III.37: Receiver crossing points.

III.E.2 Numerical simulation description

The numerical simulation of the receivers is based on the model presented in the preceding sections. A C-program is used to calculate the receiver characteristics from the input parameters. The input parameters are given in Table III.4, and the constants used in the analysis are given in Table III.5.

A photodiode capacitance of 250 fF is used on the assumption that the photodiode is implemented on-chip in standard CMOS, as described in Section II.D. This value of 250 fF gives a photodetector of reasonable size – approximately 60 μm diameter for the N-Well to P-Substrate photodiode or 25 μm diameter for the P+ to N-Well photodiode in the 0.35 μm process. Smaller photodiodes are possible, but they would make the alignment of the free-space optical system or the coupling from a multimode fiber very difficult.

The C-program loops over all values of the input parameters. For each

Table III.4: Input parameters.

Parameter	Description	Limits
L	CMOS technology (L_{min})	0.8, 0.5, 0.35, 0.1 μm
N	Number of stages in TIA	1,3
P	Number of stages in VA	0,1,2
V_b	Bias voltage	$V_{tn} + 0.1$ to $\frac{V_{dd}}{2}$
W_1	Width of gain stage NMOS M1	$1\mu m$ to $1000\mu m$
W_3	Width of gain stage NMOS M3	$1\mu m$ to W_1
DW_2	Width of decision circuit PMOS M2	$1\mu m$ to $1000\mu m$

possible combination of parameters, the program first calculates the feedback resistance necessary to produce a maximally flat magnitude response. The combinations of parameters for which no MFM solution can be found are discarded. If a combination of parameters has two MFM solution, both are calculated and recorded. The program then calculates the bit-rate, optical power, electrical power, and input equivalent noise power for the MFM solutions. Figure III.38 shows the optical power for receiver parameters over the entire range of values, for the 0.35 μm CMOS process.

The program then sorts the receivers according to the performance metric selected: optical power or total power. For each bit-rate, the receiver which minimizes the performance metric is found and recorded. For example, in Figure III.38 the optimization result would be the receivers on the bottom right of the scatter plot, if the performance metric were optical power.

Finally, another program is used on the generated list of optimum receiver parameters to create HSPICE decks. HSPICE simulations are then run on the optimized receivers to verify the receiver performance predicted by the model. The template HSPICE deck is shown in Section III.G.

Table III.5: Constants used in analysis.

Parameter	Description	Value
$t_{r,in}$	Input signal rise time	$2.2\tau_{min}$
C_{pd}	Photodiode capacitance	250 fF
R_{pd}	Photodiode responsivity	50 %
I_{dark}	Dark current	5 nA
Γ	Gamma for transistor noise	2

III.E.3 Optimization Results

The results of the optimization for minimum optical power in 0.35 μm CMOS are plotted in Figure III.39. This graph shows the electrical power, optical power, and input equivalent noise power versus bit-rate for the optimized receivers. Also indicated on the graph is the receiver configuration, N+P, of the optimized receivers. Note that each receiver configuration is optimum over a range of bit-rates, except the 3+0 and 3+1 configurations which are not optimum at any bit rate. This matches the prediction based on constant gain-bandwidth given in Section III.E.1.

The (1+0) configuration is optimum between 2 Gb/s and 1.7 Gb/s, requiring an optical power greater than -2.5 dBm. The (1+1) configuration is optimum between 1.4 Gb/s and 1.7 Gb/s, with an optical power requirement between -7 dBm and -2.5 dBm. Next, (1+2) receivers are optimum from 850 Mb/s and 1.4 Gb/s, and have optical power requirements from -20 dBm to -7 dBm. Finally, the (3+2) configuration is optimum below 850 Mb/s, and has an optical power requirement less than -20 dBm.

When these transition points are fit to the constant gain-bandwidth model in Section III.E.1, the gain-bandwidth product for the 0.35 μm CMOS technology is found to be approximately 16.5 GHz. This value of GBW fits the (1+0) to (1+1) transition bit-rate and the (1+1) to (1+2) transition bit-rate, but it underestimates the transition bit-rate from (1+2) to (3+2) to be about 600 MHz, instead of the 850 MHz found from the numerical simulation. This is due to the simplification of

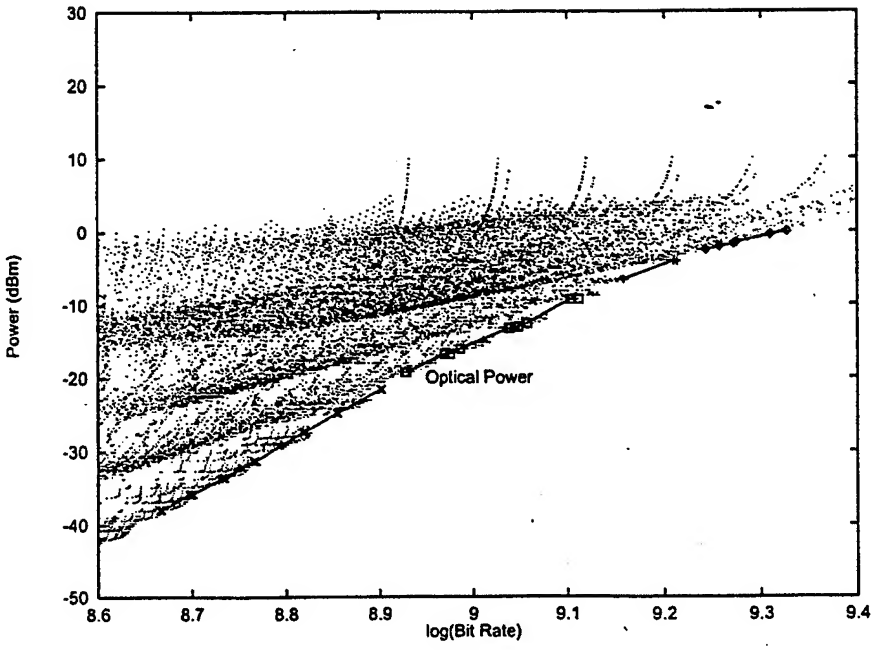


Figure III.38: Scatter plot of receiver performance, across the range of parameters, for L=0.35 μm CMOS. Optimum performance is at the right edge of the diagram.

assuming a constant gain-bandwidth. The actual gain-bandwidth is a function of bias voltage and is modified by short-channel effects. These non-idealities, absent from the constant gain-bandwidth model, are captured by the MOSFET model presented in Chapter II, which is used in the receiver model presented in this chapter.

As seen from the graph, the power dissipation P_d of the optical power optimized receivers are in the 20 to 70 mW range. Also important is that the input equivalent noise power is at least an order of magnitude smaller than the optical power requirement, except at the slowest bit-rates considered. This indicates that the bit-error rate due to receiver noise is insignificant and that this noise is not the dominant factor in determining the sensitivity of the high-speed receivers considered in this analysis. The sensitivity is determined by the gain-bandwidth of the amplifiers and the voltage swing required by the digital logic which follows

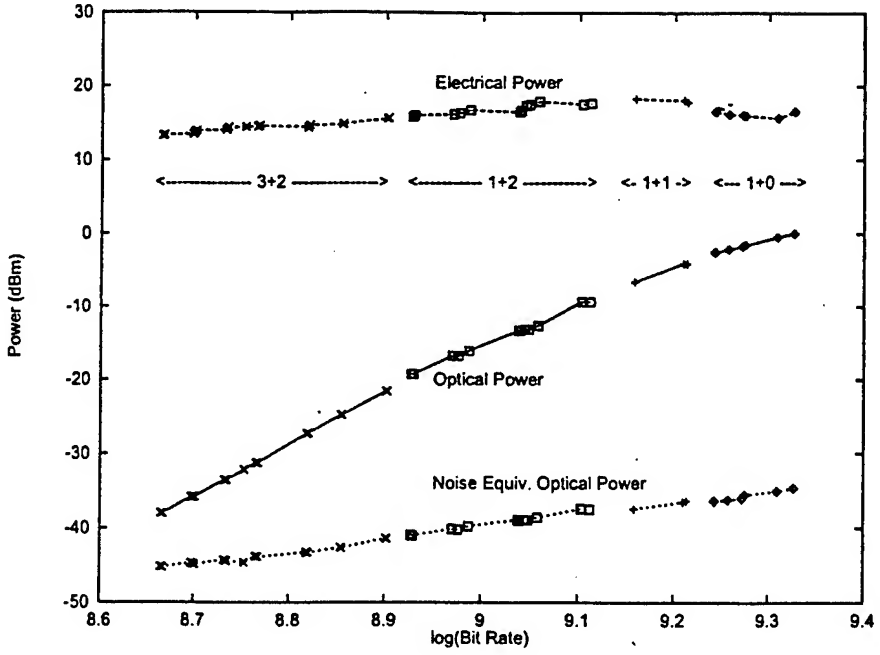


Figure III.39: Optimized receiver electrical and optical power requirements for L=0.35 μm CMOS. Optimum receiver configuration is given as N+P, where N is the number of stages in the TIA, and P is the number of stages in the voltage amplifier.

the receiver.

It is clear that these receivers are expensive to operate, from an electrical power and thermal management point of view. If an opto-electronic IC contains both receivers and transmitters, it may be more appropriate to minimize the total power dissipation in a link. This should include the power dissipation in the transmitter circuit as well. Let η represent the electrical to optical power conversion efficiency of the transmitter, including the efficiency of the optical system. Multiplying η by the optical power gives an equivalent electrical power required at the transmitter. The total power dissipated in a link is then given by:

$$P_{total} = P_d + \eta P_o \tag{III.119}$$

The solution to III.25 can be written:

$$R_f = \frac{R_o}{[1+(A_v+1)y]^2}\left[A_v x - 1 \pm \sqrt{(A_v+1)[(A_v-1)x^2 - 2x - (x+1)^2(2y+(A_v+1)y^2)]}\right] \quad \text{(III.28)}$$

If we assume $y = 0$, $A_v \gg 1$ and $x \gg \frac{2}{A_v^2}$, then the solution can be simplified to:

$$R_f = 2A_v x R_o \quad \text{(III.29)}$$

This simplified solution can be written in terms of the open-loop poles of the TIA as:

$$p_{out} = 2A_v p_{in} \quad \text{(III.30)}$$

where the open-loop poles are:

$$p_{in} = \frac{1}{R_f C_{in}} \quad \text{(III.31)}$$

$$p_{out} = \frac{1}{(R_o \parallel R_f)C_{out}} \quad \text{(III.32)}$$

Thus, if the assumptions hold, the feedback resistor is chosen such that the open-loop poles are separated by a factor of twice the gain. This is an often cited criteria in receiver design papers (see for example [40]). Unfortunately, the simplified solution can lead to significant errors when the gain is not large, as is the case with the receivers studied here. For this reason, Equation III.28 is used in this analysis for the one-stage TIA.

The low-frequency transimpedance of the one-stage TIA is found from Equation III.15 to be:

$$Z_f = \frac{R_f - g_m^{-1}}{1 + A_v^{-1}} \quad \text{(III.33)}$$

and the 10%-90% risetime of the one-stage TIA, when the transfer function is maximally flat, is

$$t_r = \frac{2.2\sqrt{2}}{2\alpha} \quad \text{(III.34)}$$

The two poles are located at $p_{1,2} = -\alpha \pm i\alpha$, where

$$\alpha = \frac{C}{D} \quad \text{(III.35)}$$

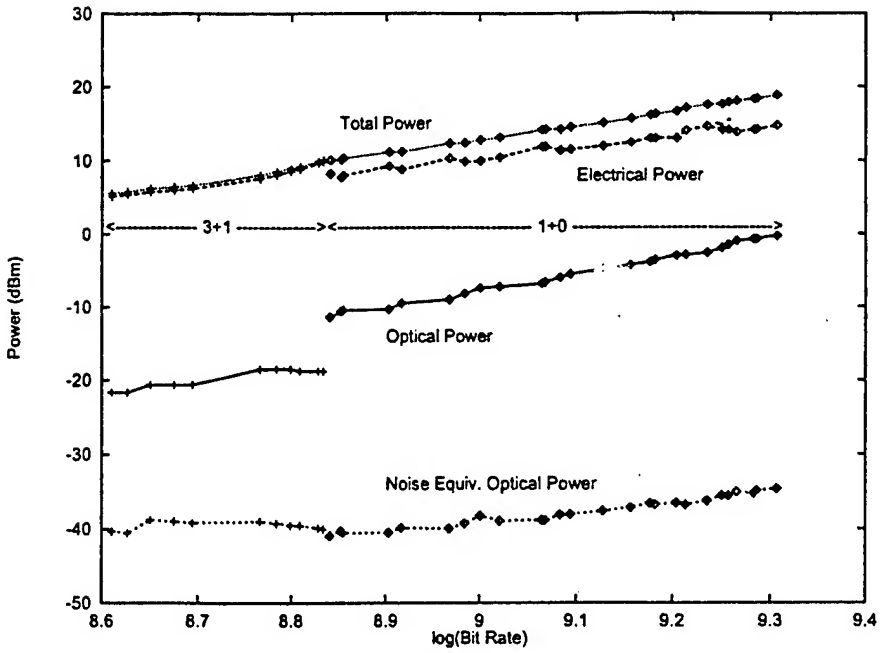


Figure III.40: Optimized receiver electrical and optical power requirements for L=0.35 μm CMOS. Optimum receiver configuration is given as N+P, where N is the number of stages in the TIA, and P is the number of stages in the voltage amplifier.

If the characteristics of the transmitter are known in greater detail, it is possible to replace the constant η with $\eta(P_o)$, where the function captures any non-linear dependence of power efficiency on optical power. In this chapter, a constant value of $\eta = 50$ is assumed, i.e. the transmitter consumes 50 mW to produce an optical power at the receiver of 1 mW. This is a reasonable (maybe optimistic) assumption given the efficiency of obtainable laser diodes and the losses expected in a relatively complex optical system. This issue is investigated in more detail in Chapter V.

The results of the optimization for minimum total power in 0.35 μm CMOS are plotted in Figure III.40. This graph shows the electrical power, optical power, input equivalent noise power, and total power versus bit-rate for the

optimized receivers. Unlike the optical power optimization results, only two configurations are optimum under total power minimization. For bit-rates above 700 MHz, the (1+0) receivers are optimum, with total power requirements from 10 mW to 80 mW and optical power requirements from -10 dBm to 0 dBm. Below 700 MHz, the (3+1) receivers are optimum, with total powers from 3.5 mW to 10 mW and an optical power requirement of about -20 dBm. Note that the electrical power requirement is smaller than that found in the optical power optimization – below 30 mW for the (1+0) receivers and below 10 mW for the (3+1) receivers – but that the optical power requirement is higher. This is because the total power optimization sacrifices optical power for lower electrical power. The (1+0) receivers are optimum over a wider range of bit-rates because the added electrical power cost of additional stages outweighs the optical power reduction gained. At 700 MHz, the (3+1) receivers are optimum because the three-stage TIA can be used at lower bit-rates with much smaller transistor sizes, and thus smaller electrical power, than the one-stage TIA. However, the additional voltage amplifier stage is needed to buffer the output of the three-stage TIA, so that it is not loaded down by the decision circuit capacitance. The input equivalent noise power is in all cases at least two orders of magnitude less than the optical power.

It should be noted that different values of η give different optimization results. In particular, for very large values of η (i.e. very inefficient transmitters), the total power optimization reduces to the optical power optimization described above. For a very small value of η, the optimization reduces to a minimization of the receiver electrical power dissipation.

Figure III.41 summarizes the results of the two optimizations by casting the results in terms of energy per bit. The curves marked "A" in the graph are for the optical power minimization, and give the optical and electrical energy per bit. The curves marked "B" in the graph are for the total power minimization, and give the optical and total energy per bit.

This graph clearly shows how the optical energy per bit can be traded off

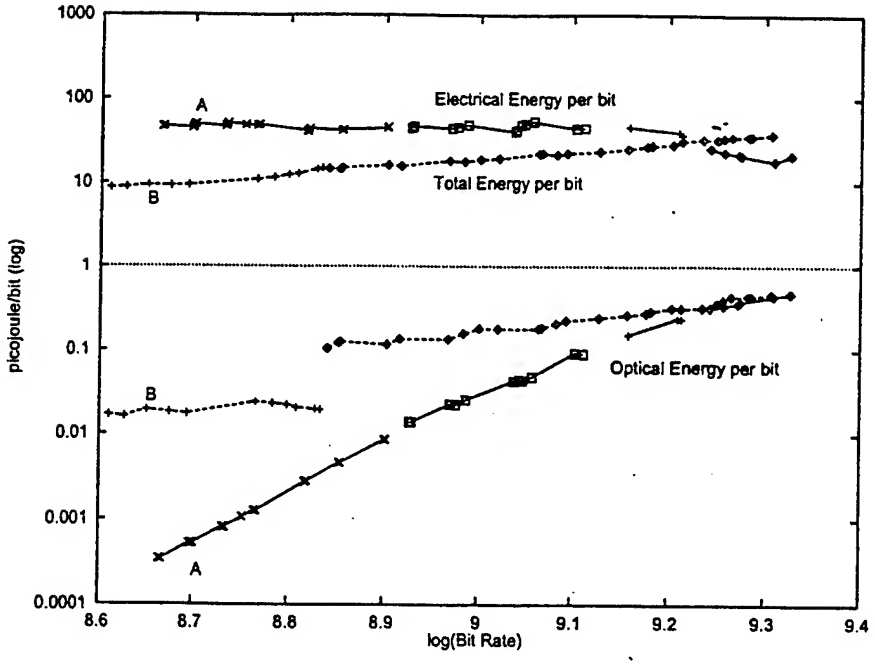


Figure III.41: Energy per bit.

to reduce the total energy per bit. At lower frequencies, the total energy per bit is reduced by 5 times by allowing the optical power to increase by approximately one order of magnitude. At the fastest bit rates, the results from the optical and total power optimizations merge. This is because fewer combinations of parameters produce receivers that operate at the highest speeds. At above 1.5 Gb/s, the optical energy per bit becomes a significant portion of the total energy per bit (depending on the value of η). This explains why the electrical energy per bit for the "A" curve drops below the total energy per bit for the "B" curve.

Also evident is that the energy per bit increases with increasing bit-rate. For the 0.35 μm example, the slope of the total energy per bit versus bit-rate is approximately 1 decade/decade. Of course, this result is only valid for the high bit-rates considered here. At much lower bit-rates, different circuit designs must be used which would have different energy/speed tradeoffs. However, it does indicate that given a data throughput requirement in $bits/sec$, the total power is minimized

by using many slow links instead of fewer fast links. However, this conclusion ignores many important aspects, such as latency, optical system complexity, routing resources, and design granularity, which might force a system designer to choose a higher bit-rate. It is for this very reason that this analysis does not attempt to present one optimized receiver design, but instead a family of designs.

Figure III.42 shows how the optimized feedback resistor value varies versus bit-rate, for optimized optical power and optimized total power receivers. It is seen that the receivers optimized for minimum optical power use a larger range of feedback resistance values. At the highest bit-rates, the feedback resistance is the same for the two optimizations, because at the limits of the gain-bandwidth of the technology there is no other design choice but to minimize the feedback resistance. Below this point, however, the optical power optimization limits the feedback resistance and adds gain stages to achieve higher sensitivity. In comparison, the total power optimization does not add gain stages, due to their extra power consumption, and instead increases the feedback resistance. At low bit-rates, when no more stages can be added, the optical power optimization increases the feedback resistance to a much larger value than that used in the total power optimized receivers. In order to use this high value of feedback resistance, the optical power optimization allows the gain stages to burn more electrical power. This is in contrast to the total power optimization, where a smaller number of stages is used and a smaller feedback resistance is used, thus increasing the speed and allowing the electrical power component to be reduced. Of course, this is with the penalty of reduced optical sensitivity.

So far we have only considered the case where $\eta = 50$ in the total power equation. Figure III.43 shows how the total energy per bit depends on η, for five different bit-rates. Also indicated is the optimum receiver configuration at each point, by the choice of the plot symbol.

As the transmitter and/or optical system becomes more and more efficient (i.e. $\eta \rightarrow 1$), the energy per bit is reduced, and it's dependence on bit-rate is also

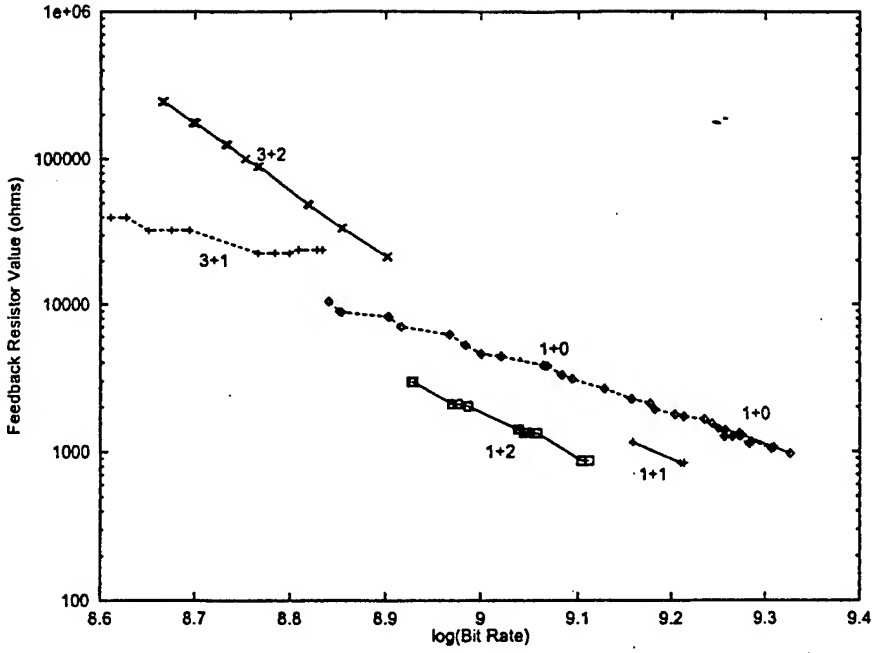


Figure III.42: Feedback resistor values for optimized receivers in 0.35 μm CMOS. The solid line is for receivers optimized for minimum optical power, and the dashed line is for receivers optimized for total power.

reduced. The optimum receiver configuration for efficient transmitters (toward the left of the graph) is 1+0 and does not change versus bit-rate. For inefficient transmitters/optical systems (i.e. $\eta \rightarrow \infty$), the situation is reversed. As expected, the energy per bit increases as more power is required to provide the same optical power to the receiver. The inefficiency also increases the dependence of the energy per bit on the bit-rate. This is because the optical source inefficiency amplifies the impact of the larger optical powers required to operate at higher bit-rates, and because higher power receivers are found to be optimum due to their higher sensitivity. Unlike the efficient case, the optimum receiver configuration is strongly dependent on the bit-rate for inefficient optical sources.

Figure III.44 shows the impact on energy per bit of reducing the photodiode capacitance from 250 fF to 50 fF, as might be obtained with a flip-chip

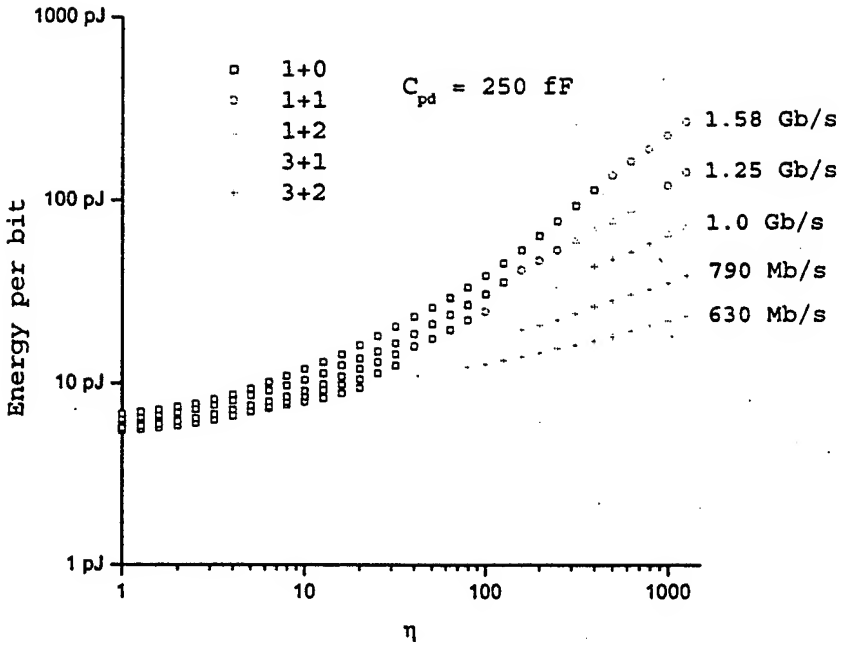


Figure III.43: Energy per bit and optimum receiver configuration at different bit rates, for different values of η, in 0.35 μm CMOS. The optimum receiver configuration is indicated by the symbol at each point.

bonded MSM detector. The energy per bit curves shift downwards, and the range over which the 1+0 receiver is optimum is extended to $\eta > 100$. For efficient transmitters, the energy per bit is reduced about 1.5 times; for inefficient transmitters, the reduction is greater than 2 times at the highest bit-rate. This improvement is not proportional to the reduction in the photodiode capacitance because the receiver input capacitance is in parallel with the photodiode capacitance. The maximum bit-rate where three-stage TIA receivers are optimum is also reduced. The optimum receiver configuration trends are the same, however.

III.E.4 Comparisons to electrical interconnects

In standard digital CMOS the energy per bit is given by $\frac{CV_{dd}^2}{2}$, where C is the capacitance of the switching nodes. From Figure III.41, the total optimized energy per bit (with $\eta = 50$) in 0.35 μm CMOS at 1 Gb/s is 19 pJ/bit. This corresponds to a switching capacitance of 3.5 pF. To roughly compare this to an off-chip electrical interconnect, assume the simplest case of an electrical output pad driver consisting of a large CMOS inverter driving the output pad and ESD parasitics, bonding wire, output package pin, PCB electrical trace, input package pin, bonding wire, and input pad and ESD parasitics, as shown in figure III.45. The total capacitance of the interconnect, $2(C_{ESD} + C_{pin} + C_{pad}) + C_{trace}$, must be equal to 3.5 pF for this electrical interconnect to provide an equivalent energy per bit as that of the optimized optical interconnect. Since $C_{pad} + C_{ESD}$ alone is typically about 10 pF, it is obvious that reaching this small of a capacitance would be nearly impossible for the off-chip electrical interconnect. Even for on-chip electrical interconnects, where only the metal routing capacitance is a factor, a rule of thumb is 1 pF per mm metal line. Thus the 3.5 pF equivalent capacitance of the optical interconnect corresponds to a 3.5 mm wire route, which is relatively small considering the $> 1\ cm^2$ die sizes of modern ASICs.

This is not meant to be the final word on the comparison between optical and electrical interconnects, which has been addressed in great detail in the lit-

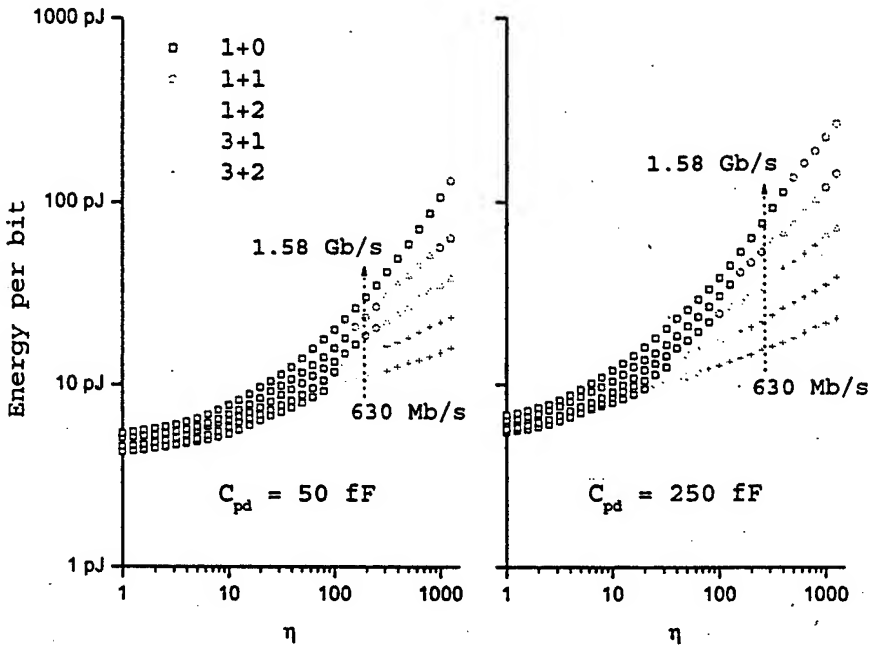


Figure III.44: Comparison of energy per bit and optimum receiver configuration for two different photodiode capacitances, 50 fF and 250 fF.

erature. There are many circuit and architectural choices for implementing more efficient electrical interconnects. The interested reader is referred to the following references for more detailed comparisons: [66], [67], [68], [69], [4].

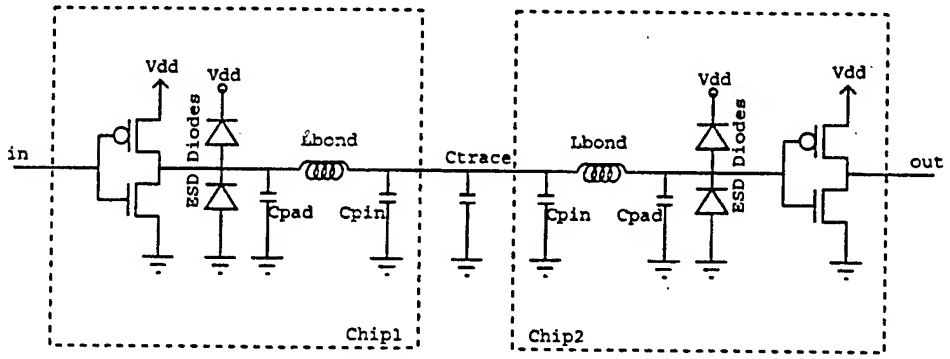


Figure III.45: A typical CMOS electrical interconnection between Chip1 and Chip2.

III.E.5 HSPICE Simulation Comparison

To verify the results of the receiver model and optimization, the optimized receivers were simulated with HSPICE. The template HSPICE deck, given in Section III.G, was filled in automatically by the receiver optimization program. The simulation used a current source to model the photogenerated current from the photodiode, in parallel with the photodiode capacitance. The amount of photocurrent used in the simulation was filled in by the optimization program to match the predicted optical sensitivity. After simulation, the voltage signal at the input to the decision circuit was measured to verify that the predicted voltage swing was being achieved with this photocurrent. The rise and fall times at the output of the decision circuit were also measured to determine the maximum bit-rate of the receiver. The photocurrent stimulus, which consisted of low and high-speed switching rates, was scaled to the predicted bit-rate. This allowed the simulation to exercise the receiver at the maximum predicted bit-rate, and to also check the response to long strings of ones and zeroes. The power dissipation was also

measured.

An example of an eye-diagram produced by the simulation is shown in Figure III.46. Shown in this figure is the voltage at the input to the receiver, at the input to the decision circuit, at the output of the decision circuit, and at the output of the Schmitt trigger.

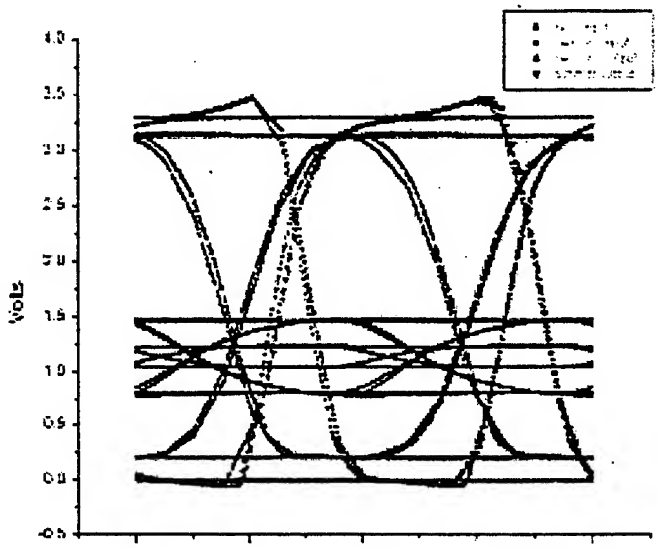


Figure III.46: Simulated eye diagram for a 0.35 μm CMOS receiver.

Figures III.47 and III.48 show the results of the HSPICE simulations and of the receiver model, for receivers optimized for minimum optical power and for receivers optimized for minimum total power ($\eta = 50$) in 0.35 μm CMOS. These figures graph the electrical power dissipation versus the optical power requirement for six different receivers of each optimization type. Both figures demonstrate that the model accurately predicts the electrical power dissipation of the receivers to within 1 dBm in all cases.

Figures III.49 and III.50 also show the results of the HSPICE simulations and of the receiver model; these figures graph the optical power requirement versus bit-rate. For the simulation results, the bit-rate has been determined by measuring

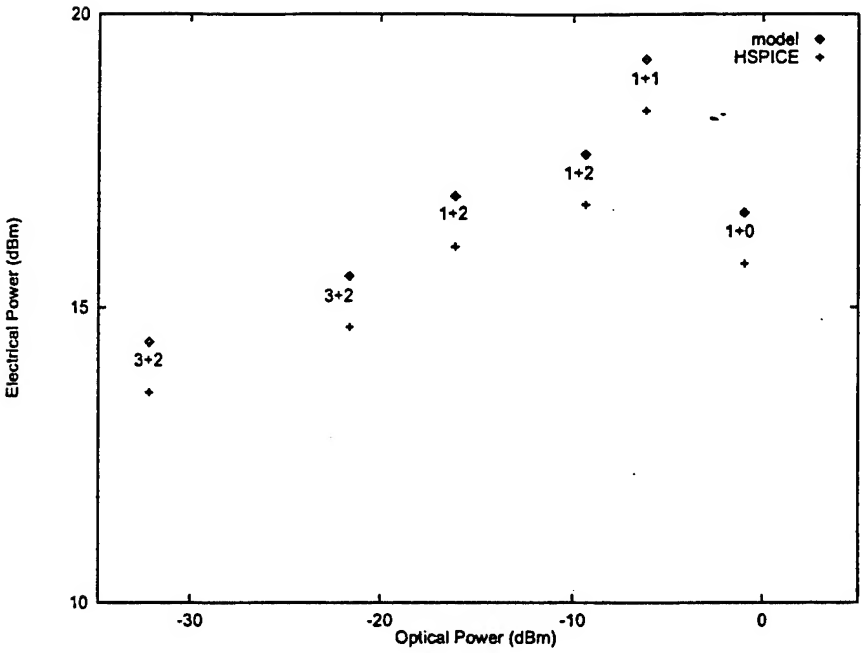


Figure III.47: Comparison of HSPICE results and model of electrical power dissipation versus optical power requirement, for receivers optimized for optical power in 0.35 μm CMOS.

the signal rise-time at the output of the decision circuit, and using Equation III.65. These graphs show that the model appears to underestimate the maximum bit-rate of the receivers. This inaccuracy stems from the approximation used to model the rise-time and gain of the decision circuit, which is given by Equation III.13. In fact, in simulation the non-linear large signal operation of the decision circuit, as opposed to the linear small signal operation of the receiver gain stages, can cause it to shorten the total accumulated rise-time through the receiver stages instead of adding to it. The model presented here uses a conservative estimate of the decision circuit gain. Better accuracy in predicting the simulated bit-rate could be achieved with a more accurate model of the decision circuit, with the drawback that such a model would complicate the model by requiring more fitting parameters.

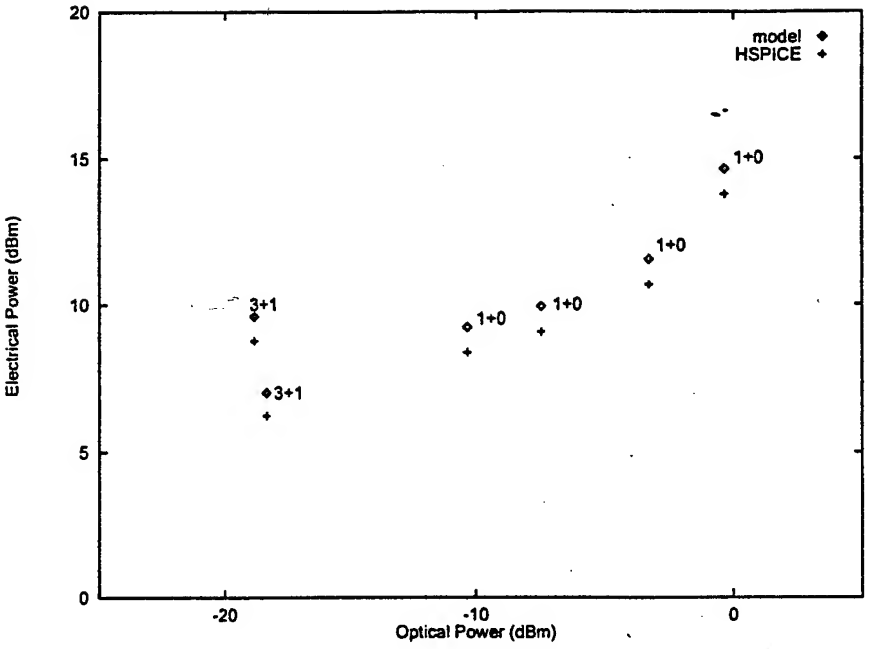


Figure III.48: Comparison of HSPICE results and model of electrical power dissipation versus optical power requirement, for receivers optimized for total power in 0.35 μm CMOS.

III.E.6 Technology Comparison

All of the results presented to this point have been for receivers in a 0.35 μm CMOS process. At the time of writing, 0.35 μm is a modern but mature technology with high availability and commodity pricing. The next chapter will describe the characterization of a receiver test chip fabricated in this process. However, to provide a complete picture of receiver performance requires examining how the receivers scale with the CMOS technology. It has been predicted that maintaining the performance of analog circuits in deep-submicron technologies will be difficult, as short channel effects come to dominate, and as the threshold voltage becomes a larger percentage of the supply voltage. Deep-submicron technologies are more expensive to manufacture, resulting in higher wafer costs, which is offset by the smaller die sizes possible with the smaller technology line-widths. However,

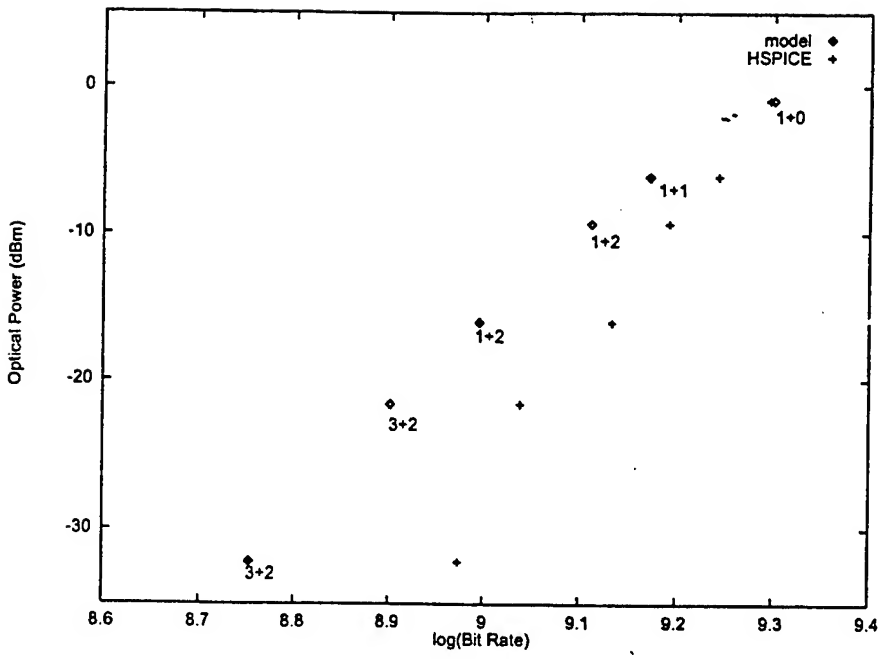


Figure III.49: Comparison of HSPICE results and model of optical power versus bit-rate, for receivers optimized for optical power in 0.35 μm CMOS.

analog circuits may not scale well, resulting in higher die costs. If the performance increase is not significant, the move to a more aggressive technology may not be warranted.

Using the MOSFET model parameters presented in Section II.A, the receiver optimization was run for the 0.5 μm (high V_t), 0.5 μm (low V_t), 0.35 μm, and 0.1 μm CMOS technologies. Figure III.51 gives the optical and electrical energy per bit for receivers optimized for minimum optical power requirement. Figure III.52 gives the optical and total energy per bit for receivers optimized for minimum total power, with $\eta = 50$.

Both figures show that as the technology improves, the maximum speed increases and the energy per bit decreases. In contrast to the predictions made about analog circuits in deep-submicron, there is a clear benefit to moving the receivers to smaller line-width technologies, When optimizing for optical power,

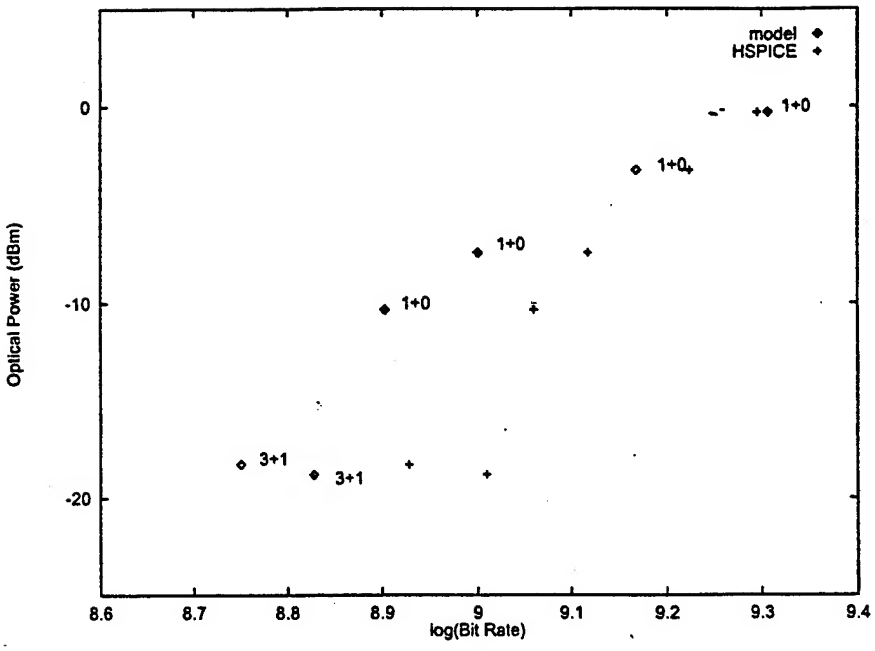


Figure III.50: Comparison of HSPICE results and model of optical power versus bit-rate, for receivers optimized for total power in 0.35 μm CMOS.

the speed increases by approximately 1.6 times when moving from 0.5 to 0.35, and 2.5 times between 0.35 and 0.1 μm. The electrical energy per bit also drops by about a factor of two between technologies. There is also a benefit, but not as large, to using a smaller V_t. This is seen in the difference between the two 0.5 μm curves. The main improvement in scaling the V_t is a speed increase of 25%. The electrical energy per bit does not improve much by scaling the V_t.

Figure III.51 also shows how the significant short-channel effects in 0.1 μm CMOS distort the curve predicted in simple constant gain-bandwidth approximation given in Section III.E.1.

When optimizing for total power, the speed gains are slightly smaller than for the minimum optical power case. From 0.5 to 0.35 is a 40% increase, and from 0.35 to 0.1 μm is a 100% increase. At lower bit-rates, where all three technologies are available, the technology scaling translates into a total energy

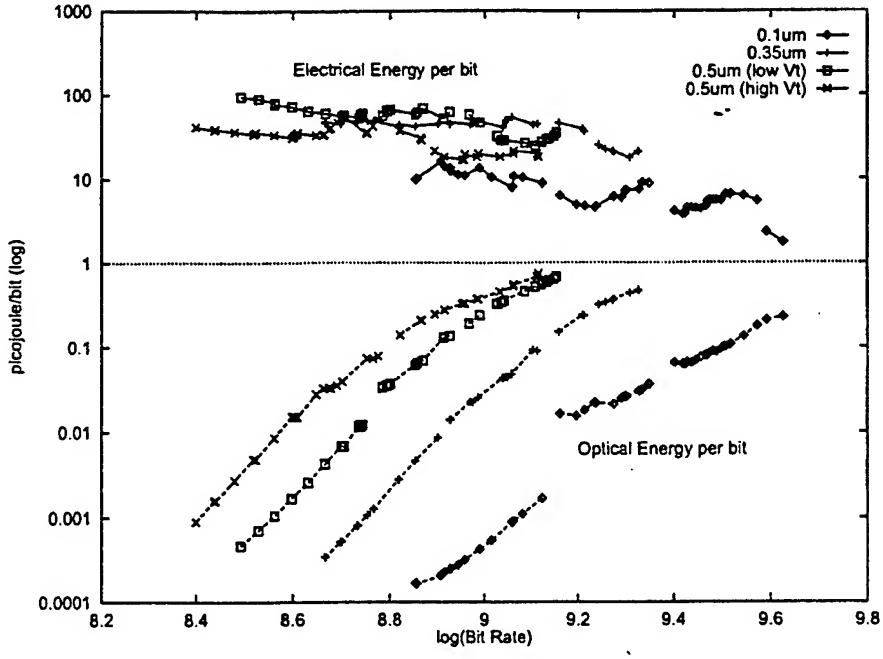


Figure III.51: Optical and electrical energy per bit for receivers optimized for minimum optical power requirement.

per bit reduction of 44% from 0.5 to 0.35, and 88% from 0.35 to 0.1 μm. The optical energy per bit decreases by a similar amount. It is interesting to note that the V_t scaling between the two 0.5 μm technologies does not make a significant difference in their performance. This is in contrast to the improvement seen in the optical power minimization case, when the V_t was reduced. The reason for this discrepancy is that scaling the V_t improves the gain of the amplifiers, but since the supply voltage is the same in both case, it does not significantly effect their electrical power dissipation. Unlike the optical power minimization, the total power minimization includes the receiver electrical power; thus the difference seen previously between the different V_t processes is greatly reduced.

One conclusion to draw from this analysis is that there may be little benefit to using advanced processes which allow for different V_t's on different transistors, unless the supply voltage is also reduced on the low-V_t circuits. This would require

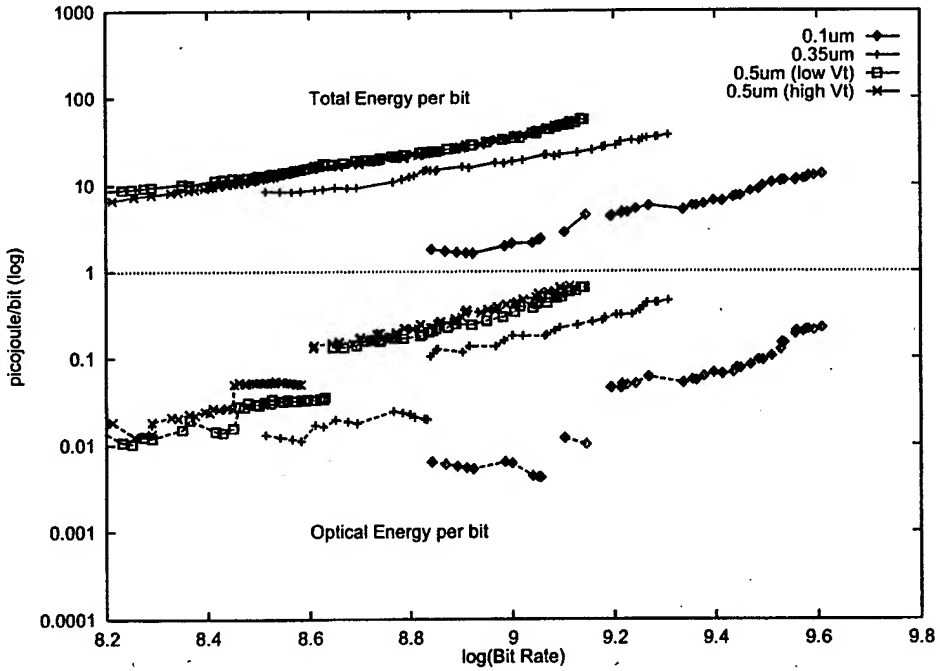


Figure III.52: Optical and total energy per bit for receivers optimized for minimum total power requirement.

multiple regulated supplies at different voltages, which would greatly complicate the system design.

Appendix IV: Experimental CMOS Receivers

IV.A Introduction

In order to experimentally verify the receiver model and optimization presented in the preceding chapter, a test chip was fabricated and tested, containing experimental receivers. The experimental receivers were tested with both electrical and optical stimulus. In addition, CMOS compatible detectors were tested and characterized.

This appendix describes the receiver test chip, and presents the schematics and layouts for the receiver test structures. The results of the electrical tests are then presented, along with a comparison to the model and simulation results. Then the optical tests are described, which make use of integrated CMOS-compatible detectors. A data coding algorithm is suggested to compensate for the long diffusion time of carriers in CMOS-compatible detectors, and the improvements when using this data coding are verified experimentally.

IV.B Receiver Test Chip

IV.B.1 Test chip overview

The receiver test chip was fabricated in 0.35 μm CMOS. This test chip contained structures to test the optimized receivers both optically (using CMOS compatible detector structures), and electrically (using a MOSFET to simulate the photocurrent from a detector).

The test chip contained 12 receivers, with six optimized for minimum optical power, and six optimized for minimum total power with $\eta = 50$. Each receiver was optimized for operation at a different bit-rate. The supply to each receiver was individually selectable, to allow for power dissipation measurements. The outputs of the receivers were multiplexed through pass transistors to the high-speed output pads. Care was taken to separate the supplies between the receivers, drivers, and the output driver, to avoid switching noise coupling back into the receiver front-end.

A PCB was also designed and fabricated. The receiver test chip was mounted on the PCB, which provided the interface cabling and electronics, supply decoupling, and terminated the high-speed SMA connections to 50 ohms. This PCB was also designed with split power planes, to minimize cross-talk between the sensitive analog supply and the noisy 50 ohm output driver supply.

Two different CMOS compatible detectors were used for optical tests. One detector used the N-Well to P-substrate junction, and the other used the P+ diffusion to N-Well junction, as described in Section II. The N-Well to P-substrate detector was expected to have high responsivity at the optical test wavelength of 850nm because of the deeper junction, but the diffusion time of carriers in the substrate was expected to degrade the speed of this detector. The P+ to N-Well detector was expected to have a very low responsivity at 850nm due to the shallow junction depth, but was expected to be fast because the N-Well would collect any carriers not generated in the depletion region of the detector. Six

of the more sensitive receivers were connected to the P+/N-Well detectors, and the remaining receivers used the N-Well/P-substrate detectors. In addition, a stand-alone detector of each type was bonded out to allow for measurement of its responsivity and calibration of the electrical tests.

A block diagram of the receiver test chip is shown in Figure IV.1.

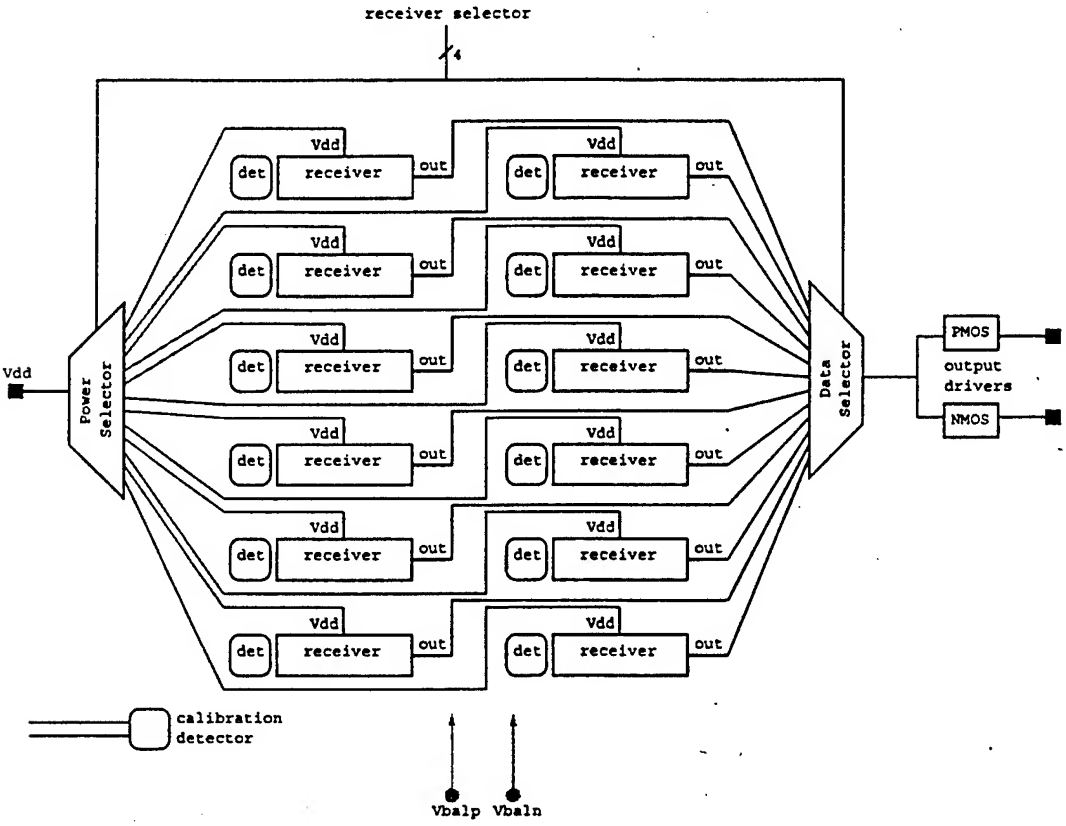


Figure IV.1: Block diagram of the receiver test chip.

IV.B.2 Receiver schematics

The model and optimization program described in Chapter III was used to find the transistor sizes and number of stages for the optimum receivers. Each receiver was optimized for operation at a different maximum bit-rate. Of the twelve fabricated receivers six receivers were tested, labeled R10, R8, R7, R4, R2, and R0.

Table IV.1: Experimental receiver design parameters.

Receiver	Optimization	Config.	R_f	A_v	design V_b	meas. V_b
R10	P_{total}	3+1	23.8 $k\Omega$	2.29	1.0	1.03
R8	P_{total}	1+0	4.6 $k\Omega$	5.62	1.1	1.11
R7	P_{total}	1+0	1.9 $k\Omega$	3.67	1.0	1.03
R4	P_{opt}	3+2	21.3 $k\Omega$	2.22	1.1	1.07
R2	P_{opt}	1+2	870 Ω	3.06	1.0	0.96
R0	P_{opt}	1+0	1.1 $k\Omega$	3.52	1.1	1.08

Receivers R10, R8, and R7 were optimized for minimum total power with $\eta = 50$. Receiver R4, R2, and R0 were optimized for minimum optical power.

Table IV.1 gives the design parameters for the tested receivers. Listed in this table are: the receiver configuration (given as N+P, where N is the number of gain stages in the transimpedence amplifier, and P is the number of gain stages in the voltage amplifier), the feedback resistance R_f, the unloaded gain-stage gain A_v, and the modeled and experimentally measured values of the bias voltage V_b. Table IV.4 shows the performance of the receivers as predicted by the model. Also shown in this table is the experimentally measured performance, which is described below.

The inputs to all six of the tested receivers were connected to N-Well/P-Substrate photodiodes. These on-chip photodiodes were used to simulate the photodiode capacitance for the electrical tests, and were stimulated with an optical signal for the optical tests. The photodiode capacitance was designed to match the value of 250 fF used in the optimization, which yielded a 60 μm diameter detector.

The other six receivers, which were connected to P+/N-Well photodiodes, did not operate properly due to self-oscillation. Because of a layout oversight, the N-Well of these photodiodes was connected directly to the supply rail of the receiver, instead of to a quiet reference voltage. This allowed the supply noise to couple directly through the detector capacitance onto the input node, which is the

Table IV.2: Experimental receiver transistor parameters.

Receiver	Mbp	Mbn	M1	M2	M3	Mfp	Mfn	Md1	Md2
R10	1.8/3.0	1.8/0.6	7.9/0.35	3.6/0.35	2.8/0.35	2.4/0.5	1.4/1.0	28.8/0.35	9.2/0.35
R8	4.0/1.0	3.0/0.6	20.0/0.35	11.0/0.35	2.0/0.35	5.2/0.35	3.0/0.5	32.2/0.35	16.1/0.35
R7	8.0/1.0	5.0/0.6	39.8/0.35	15.0/0.35	7.9/0.35	12.8/0.35	3.0/0.35	64.4/0.35	20.2/0.35
R4	1.8/3.0	1.8/0.6	22.4/0.35	15.2/0.35	7.9/0.35	1.8/0.5	2.2/1.0	45.5/0.35	22.6/0.35
R2	1.8/1.0	1.8/0.6	100.0/0.35	39.0/0.35	25.0/0.35	32.4/0.35	6.4/0.35	81.1/0.35	25.4/0.35
R0	16.0/1.0	8.7/0.6	125.9/0.35	74.5/0.35	25.1/0.35	16.8/0.35	5.6/0.35	102.0/0.35	50.4/0.35

most sensitive node in the receiver.

The N-Well/P-substrate detectors did not suffer from this noise coupling problem. This indicates that the substrate noise was much smaller than the supply noise for the receivers. This is not surprising, given the low-impedance ground connection to the substrate, compared to the higher impedance in the supply line from the power selection transistor used to individually power each receiver. Future designs must use a separate, clean reference voltage for the detector bias.

The complete receiver schematics for the four different receiver configurations tested are shown in Figures IV.2, IV.3, IV.4, and IV.5. Table IV.2 summarizes the fabricated transistor parameters, as determined by the optimization program. All transistor dimensions in this table are in μm.

The receiver gain stage consists of transistors M1, M2, and M3. Their widths are determined by the optimization program, and their lengths are the minimum in the process, i.e. 0.35 μm. The gain stage is replicated, with its input tied to its output, to generate the bias voltage V_b. Each experimental receiver has a dedicated bias voltage generator with a dual-poly decoupling capacitor at its output. Since the bias voltage generator could be shared across multiple receivers, its power dissipation was not included in the power optimization program. To

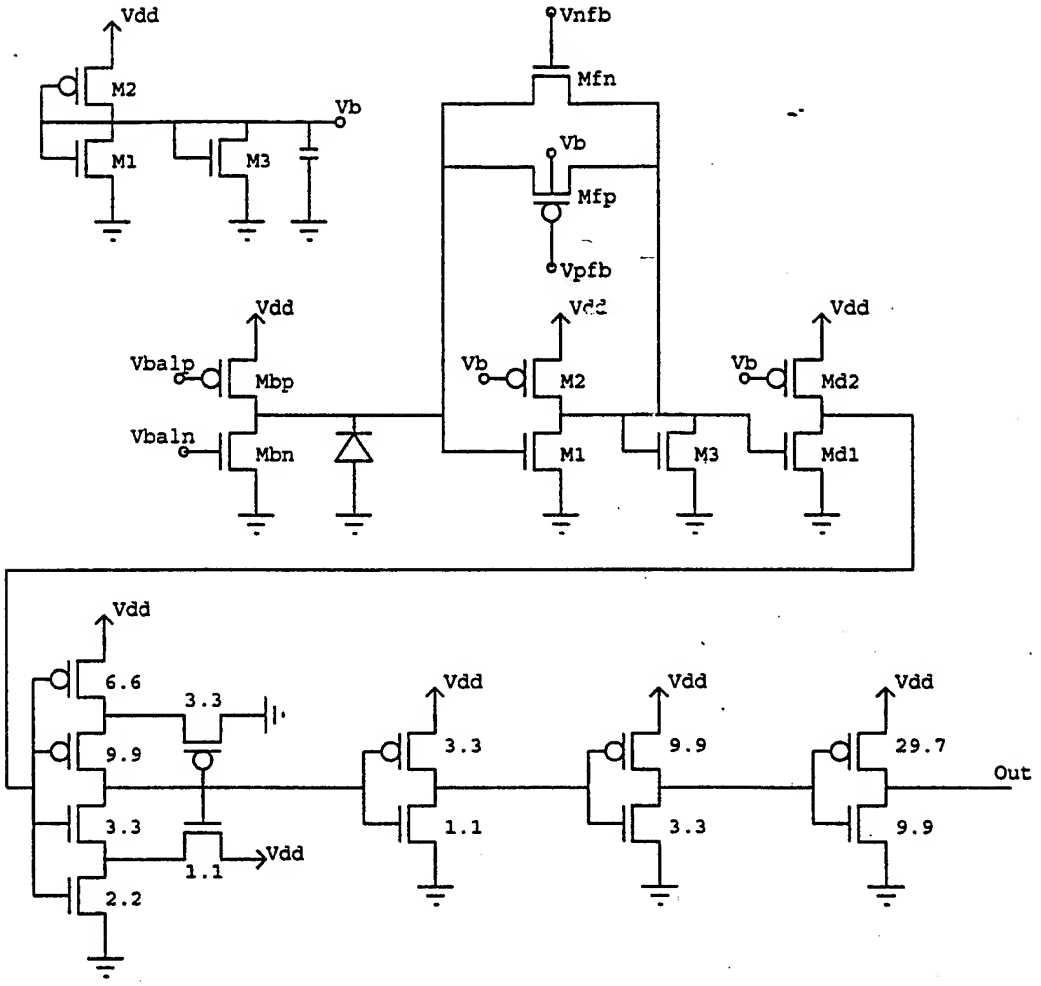


Figure IV.2: Full receiver schematic for a 1+0 receiver.

allow for comparisons between the model and the measurements, the bias generator power dissipation has been factored out of the measured total electrical power.

The decision circuit, which thresholds the receiver signal and produces the final digital voltage swings, consists of transistors Md1 and Md2. The width of these transistors is also determined by the optimization program, and the lengths are minimum.

PMOS transistor Mbp is used as a bias current-source to convert the on-off current from the detector to a symmetrical current that changes sign but has the

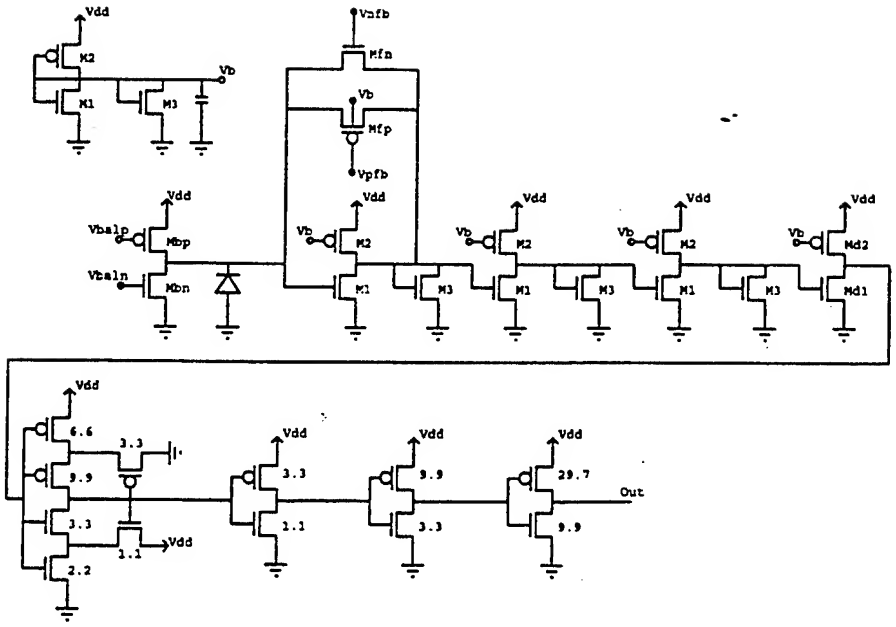


Figure IV.3: Full receiver schematic for a 1+2 receiver.

same magnitude for both 1 and 0 bits. (See Figure III.3). The length is chosen to be at least 1.0 μm, to increase the output resistance of the current-source. NMOS transistor Mbn is used as a variable current source, to simulate a photocurrent for high-speed electrical tests. During optical tests this transistor is turned off. Its length is chosen to be non-minimum (0.6 μm) to keep the output resistance of the current-source high. The dimensions of Mbp and Mbn are adjusted depending on the sensitivity of the receiver, since this determines the magnitude of the current required through these transistors.

The parallel combination of transistors Mfp and Mfn implement the feedback resistor. The sizes of these transistors are chosen to be as small as possible, to reduce the capacitance associated with the feedback resistance. The transistor dimensions are chosen using HSPICE to create the feedback resistance called for by the optimization program. When determining the sizes, the nominal bias voltages are set to $V_{pfb} = 0V$ and $V_{nfb} = V_b + 1.1V$.

Finally, the Schmitt trigger and super-buffer are implemented as de-

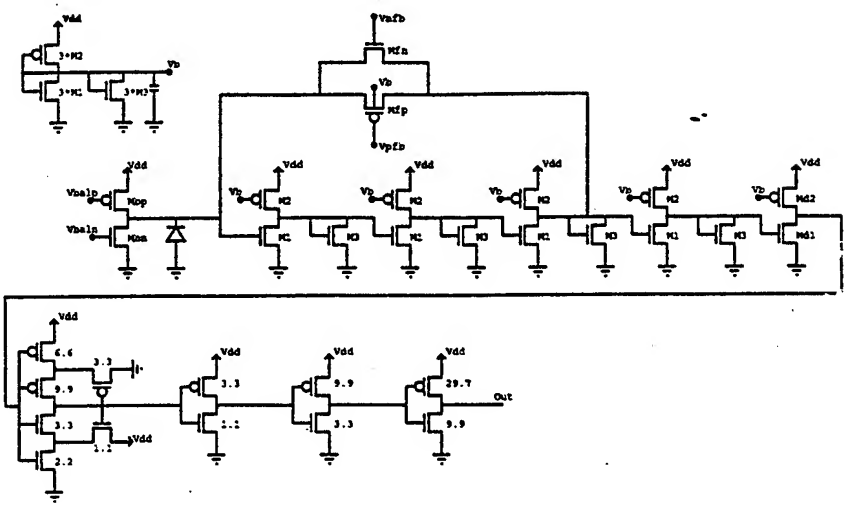


Figure IV.4: Full receiver schematic for a 3+1 receiver.

scribed in Section III.C.4. The lengths of all of the transistors in the digital buffer are the minimum 0.35 μm for highest speed.

IV.B.3 Layout

A picture of three of the fabricated receivers, along with their CMOS photodiodes, is shown in Figure IV.6. The top two receivers are connected to the N-Well/P-substrate detector. The bottom receiver uses the P+/N-Well detector. The probe pad for measuring the bias voltage V_b is shown to the right of each receiver.

The layout sizes of the six tested receivers are summarized in Table IV.3. This layout size excludes the bias voltage generator and the decoupling capacitors, but includes the digital buffer. Using the experimentally measured power dissipation, the power density for each receiver is also given in this table. These power densities are an order of magnitude or more larger than the 10 W/cm^2 density rule of thumb for an air cooled chip. To meet the 10 W/cm^2 criteria, these receivers must be surrounded by substantially lower power density circuitry, or more advanced cooling techniques must be used.

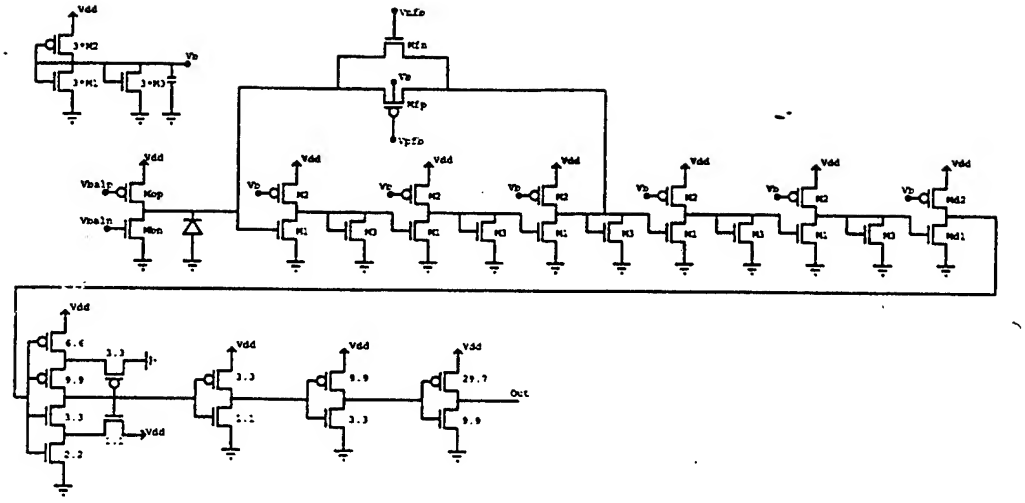


Figure IV.5: Full receiver schematic for a 3+2 receiver.

Table IV.3: Receiver layout sizes.

Receiver	Size	Power density
R10	26 μm x 142 μm	220 W/cm^2
R8	26 μm x 115 μm	264 W/cm^2
R7	26 μm x 167 μm	242 W/cm^2
R4	26 μm x 238 μm	457 W/cm^2
R2	26 μm x 457 μm	366 W/cm^2
R0	26 μm x 280 μm	397 W/cm^2

IV C Electrical tests

The receiver's performance depends in part on the speed and responsivity of the optical detector. Since one objective of the test chip was to characterize the receiver circuit performance independent of the detector, electrical tests were performed that simulated operation with a very high speed detector. The V_{baln} input, which controls the gate voltage on the Mbn transistor, was used to control the simulated photocurrent. As long as $V_{baln} < V_b + V_t$ the Mbn transistor is in saturation, and acts like a current source with a reasonably high output impedance. This criteria was easily met for the currents required by sizing the Mbn transistor appropriately. Even though not illuminated for these electrical tests, the detec-

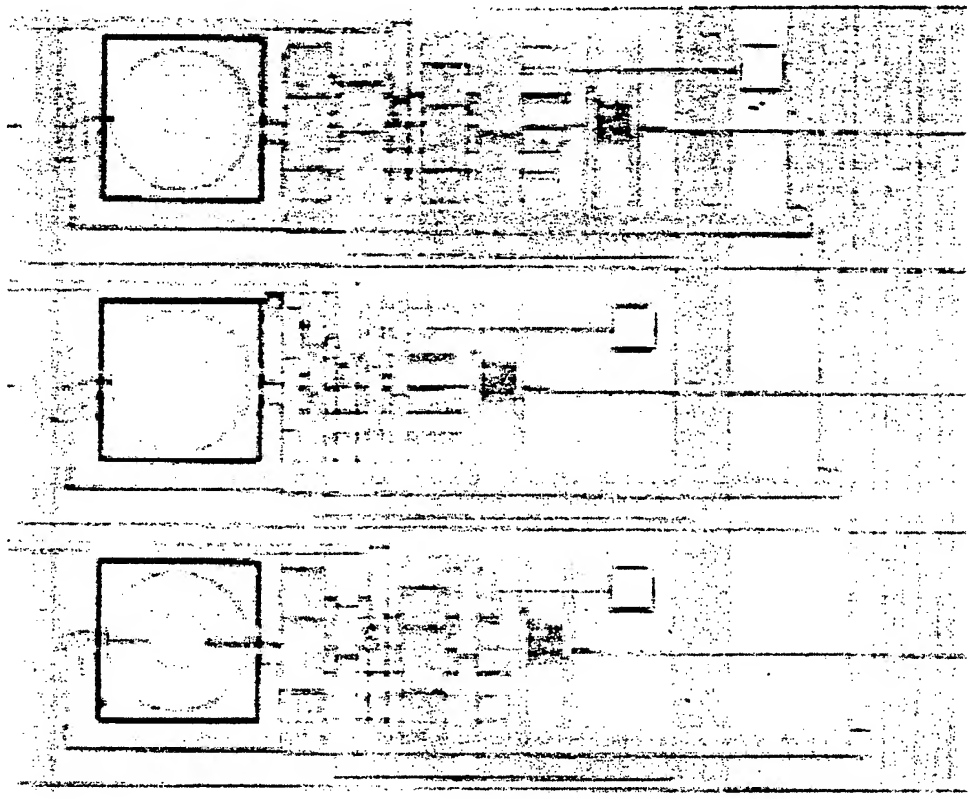


Figure IV.6: Three fabricated receivers, with photodetectors.

tor was always connected to the input node, effectively simulating the detector capacitance.

A HP 8133A high-speed pulse generator was used to generate the control voltage V_{baln}. A typical output from the pulse generator is shown in Figure IV.7. Here it is seen that the rise and fall time of the test signal is short enough to not be a limiting factor in the test set-up. The voltage swing of the signal was adjusted, along with the constant bias voltage V_{balp}, to produce the most open eye-diagram at the highest possible speed. The feedback transistor bias voltages V_{nfb} and V_{pfb} were set at the nominal values used in the simulations, as this produced the most open eye diagrams.

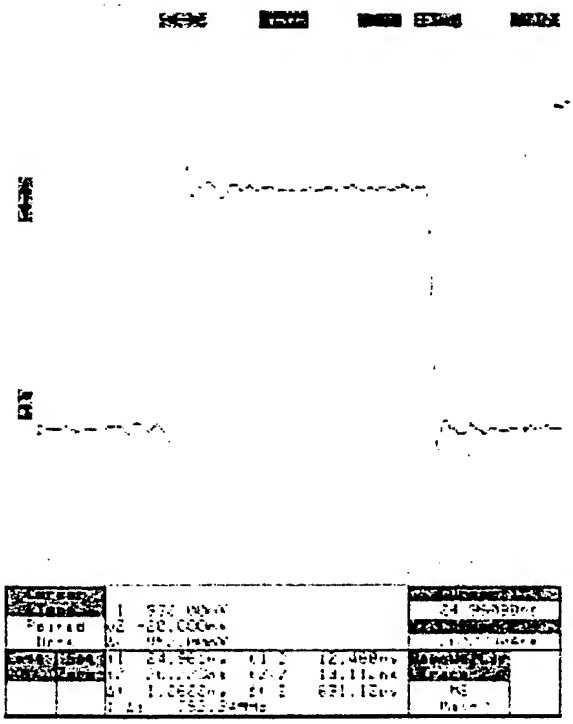


Figure IV.7: Input voltage signal from pulse generator at 622 Mb/s.

IV.C.1 Calibration of electrical source

To determine the equivalent photocurrent represented by the voltage swing of the V_{baln} signal, the receiver was tuned to its switching point with V_{baln} set to its high voltage. Then V_{baln} was set to zero, and the optical source was used to find the equivalent optical power on the detector that brought the receiver back to its switching point. Then using the calibration photodiode, the equivalent photocurrent was measured for this optical power.

The measured results for average optical power presented in Table IV.4 were found by first converting the voltage swing on V_{baln} to an equivalent photocurrent as above. The average optical power was then calculated assuming a photodiode with responsivity 0.5 A/W, as in the model.

IV.C.2 Eye-diagrams

A HP 11802B high-speed sampling oscilloscope was used to capture the eye-diagrams of the receivers. The eye-diagrams were created using a pseudo-random bit sequence (PRBS) generated by the pulse generator. The eye diagrams for all six receivers are presented in Figures IV.8 through IV.13. Also shown on the eye diagrams is a hexagonal mask at the center of the eye. This mask is used to count hits that fall within the eye center, and is based on the standard mask used for OC12 optical link testing. The mask ensures that the data is stable for at least 20% of the bit period. In all of the eye diagrams presented here, there are no hits within this mask, indicating that the eye is open and the bit error rate is low.

It is possible to create an open eye diagram and still have poor signal quality. For example, if pulses the size of a single bit are entirely lost, the eye may be open but the output data will be corrupted. To insure this was not the case, different data patterns were tried with single pulse bursts. The receivers faithfully reproduced the data patterns, indicating that the open eye diagrams represent high quality links.

The bit-error rate (BER) can be estimated from the eye diagrams by measuring the standard deviation of the distribution of the 1 and 0 values in the stable portion of the eye, and comparing this to the signal swing, in the manner described in Section III.D.8. However, this technique would find the BER of the high-speed 50 ohm output driver, not the receiver circuit. To properly use this technique, ideally the receiver signal should be tapped before the input to the decision circuit, where the thresholding occurs. Unfortunately, this is impossible due to the drive and loading requirements of the oscilloscope. Without BER test equipment, it was impossible to measure the exact BER. However, from the eye opening and lack of hits within the test mask over many thousand captured waveforms, it appears that the BER is very low – better than the 10^{-15} required for digital links.

Table IV.4: Experimental receiver measurements.

Receiver	Model				Measured			
	Bit Rate	P_{elec} mW	P_{opt} μW	P_{total} mW	Bit Rate	P_{elec} mW	P_{opt} μW	P_{total} mW
R10	670 Mb/s	9.1	13	9.75	622 Mb/s	8.12	15	8.87
R8	1 Gb/s	9.8	180	18.8	1 Gb/s	7.89	175	16.64
R7	1.5 Gb/s	14.2	473	37.85	1.1 Gb/s	10.49	460	33.49
R4	800 Mb/s	35.7	7		740 Mb/s	28.25	16	
R2	1.3 Gb/s	57.7	116		875 Mb/s	43.46	122	
R0	2 Gb/s	45.8	804		1 Gb/s	28.91	780	

Table IV.4 summarizes the results from the model and the measurements of the experimental receivers. The measured equivalent optical power matched closely the modeled optical power requirement for all six receivers. The measured electrical power dissipation was slightly lower than the modeled values, and the discrepancy was worse for receivers optimized for minimum optical power. The measured maximum speed for receivers R10, R8, and R4 matched the model well, but the other receivers were significantly slower than predicted. It is likely that the 50 ohm off-chip driver was a limiting factor at the higher speeds. Although this was not predicted by simulation, it is possible that parasitic capacitances and inductances due to the package and the PCB test board limited the maximum output speed.

The model predictions were based on nominal process parameters – as shown in Section III.D.10, process variations can have a large effect on the performance of the receivers. Another source of error is the resistance in the supply rail due to the power selection transistors. This voltage drop in the receiver supply would have the greatest affect on the highest power receivers. This might explain why the receivers optimized for minimum optical power, which used larger transistors and dissipated the most power, were slower than expected.

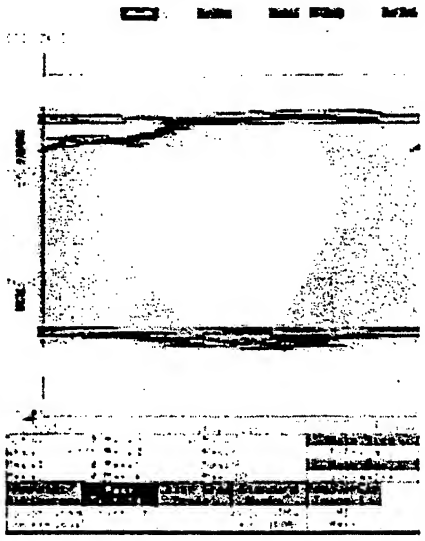


Figure IV.8: Measured eye diagram for receiver R10 at 622 Mb/s.

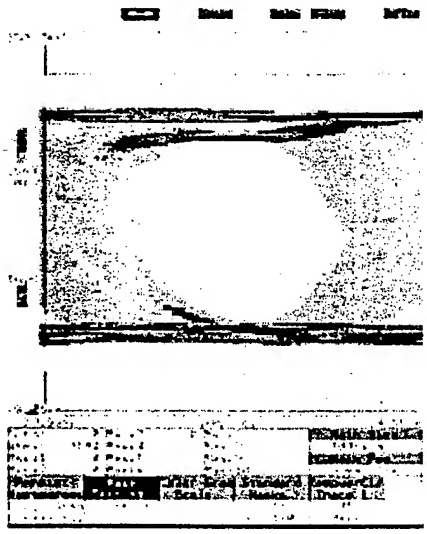


Figure IV.9: Measured eye diagram for receiver R8 at 1 Gb/s.

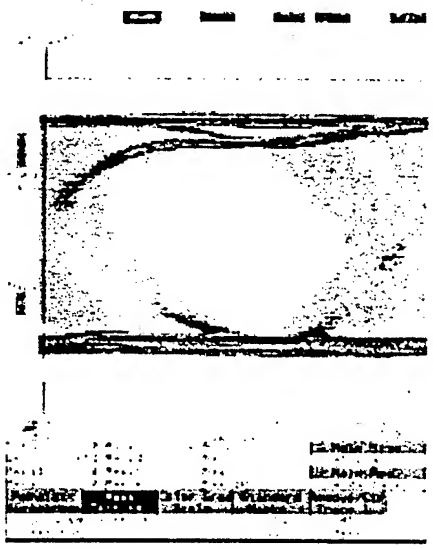


Figure IV.10: Measured eye diagram for receiver R7 at 1.1 Gb/s.

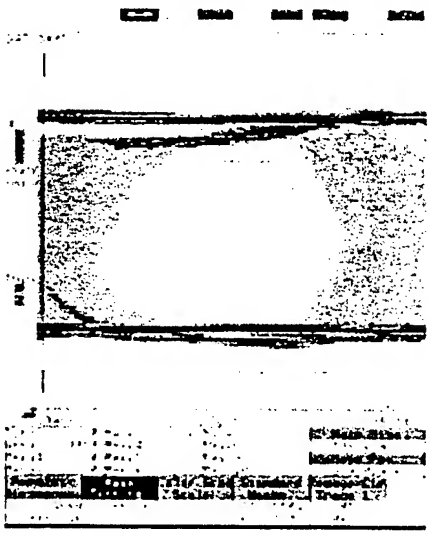


Figure IV.11: Measured eye diagram for receiver R4 at 740 Mb/s.

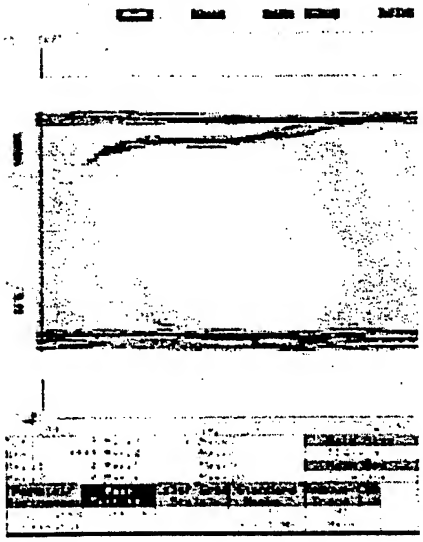


Figure IV.12: Measured eye diagram for receiver R2 at 875 Mb/s.

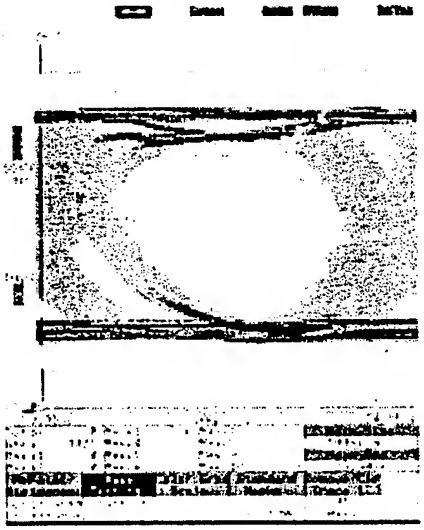


Figure IV.13: Measured eye diagram for receiver R0 at 1 Gb/s.

IV.D Optical tests

In addition to the electrical tests described above, the receiver and integrated N-Well/P-substrate photodiode were tested optically. The optical tests were performed with a commercial 850 nm diode laser module with a maximum operating bit-rate of 2 $Gbit/s$. The differential input to the laser module was driven by the high-speed pulse generator. The multi-mode fiber output of the laser module was fed to a mechanically adjustable attenuator, and then to a lensed fiber probe tip mounted in a fiber probe assembly. The attenuator was used to adjust the optical power delivered by the probe tip, from less than 1 μW to 320 μW average optical power. On the probe station, the fiber tip was aligned to the photodetector structure through the microscope. Alignment was fine-tuned during operation by adjusting the probe position to the point of maximum response.

IV.D.1 Detector responsivity and speed

The responsivity of the two photodiode structures was found using the calibration detectors, which were bonded out to pins. First, the optical power from the fiber probe tip was measured with an optical power meter. Then the photocurrent was measured from the detector, with different reverse biases, using a HP 4140B Picoamp meter. The responsivity for the N-Well/P-substrate detector was 0.46 A/W, and this value was constant for reverse biases from 0 to 2 volts. The responsivity for the P+/N-Well detector was 0.009 A/W at 3.3V reverse bias (P+ node at 0V) and dropped to 0.0081 A/W at 1.3V reverse bias (P+ node at 2V), where the N-Well was held at 3.3V. The dark current for the N-Well/P-substrate photodiode was less than 2 pA. The P+/N-Well detector had a slightly higher dark current of 60 pA.

The responsivity of the detector can be written [20]

$$\rho = \frac{\eta e}{h\nu}(1-R)\left[1-\frac{e^{-\alpha W}}{1+\alpha L_n}\right] \qquad \text{(IV.1)}$$

where η is the quantum efficiency, e is the electronic charge, $h\nu$ is the photon

energy, L_n is the diffusion length for electroncs in the substrate, α is the absorption coefficient, W is the width of the depletion region, and R is the reflection coefficient from the surface of the detector.

High speed response is obtained from carriers generated in the depletion region – the fraction of light absorbed there is $(1 - e^{-\alpha W})$. Much slower response is obtained from carriers that diffuse from deep in the substrate to the depletion region. These carriers are accounted for by the term $(1 + \alpha L_n)$. At 850 nm, the absorption length $(\frac{1}{\alpha})$ is 14 μm. The diffusion length L_n can be 100 μm or more. Considering that the N-Well depth is only several microns deep, a good portion of the absorbed light must diffuse back to the depletion region when operating at 850 nm.

The maximum possible responsivity at 850 nm, $\frac{e}{h\nu}$, is 0.69 A/W. Our N-Well/P-substrate detector with responsivity of 0.46 A/W shows a maximum loss of about 33%, due to reflections when illuminated by the fiber probe. This assumes 100% absorption and collection of the photogenerated carriers. In the layout, the passivation was cut over the photodiode in the manner used to open the pads for bonding. The thinned passivation may have helped reduce the reflection losses.

The speed of the N-Well/P-substrate detector was measured by connecting the calibration detector to the 50 ohm oscilloscope input through a bias-T. The bias-T was used to apply different reverse biases to the detector, to see how the detector speed varied with reverse bias. The oscilloscope averaging function was used to reduce the noise, since the voltages measured were less than 10 mV. Figure IV.14 shows the detector response for a square wave optical input at 150 MHz, which was used to be above the 100 MHz cut-off frequency of the bias-T. The three curves in the figure are the results for reverse biases of 0, 1, and 3 volts, with the fastest curve at 3 volts and the slowest curve at 0 volts. Table IV.5 summarizes the 10% to 90% rise times for the different bias conditions. The reverse bias condition used in the experimental receivers is set by V_b, and is approximately 1 volt.

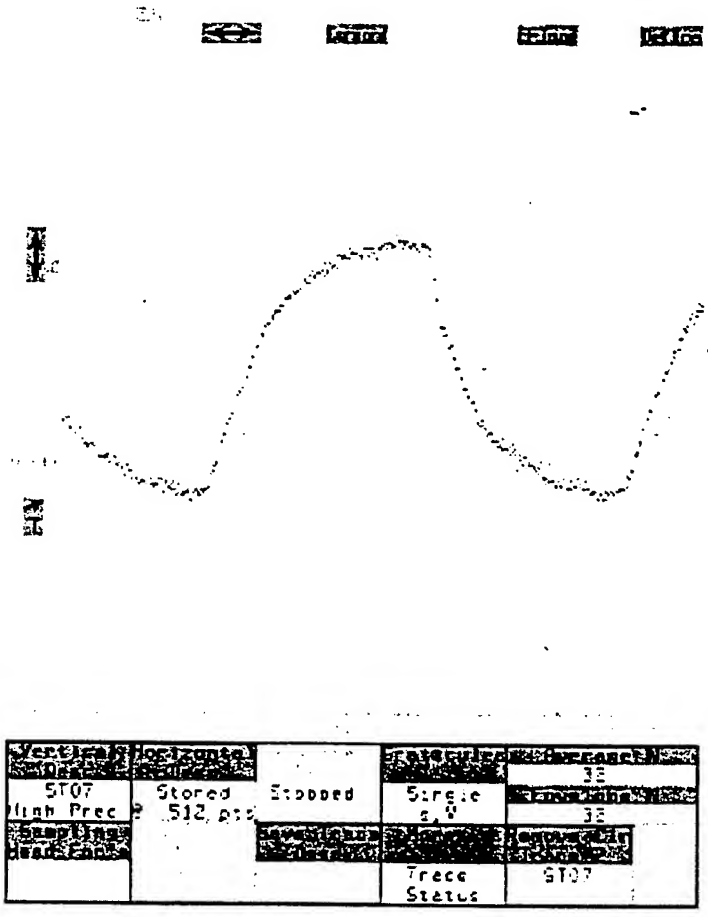


Figure IV.14: Speed of the N-Well detector, at reverse bias voltages of 0, 1, and 3 volts

Using the criteria that the rise time is 60% of the bit period (see Equation III.65) means the maximum speed possible with this detector is 285 Mb/s with a 1 volt reverse bias. The detector speed improves slightly with a larger reverse bias. This is due to the widening of the depletion region width W. Increasing the reverse bias is difficult, however, since the the substrate is tied to ground and the input to the receiver is set to V_b by the feedback.

Even if the 60% criteria is ignored, the long diffusion time of carriers generated deep in the silicon contributes to a base-line wander effect with this detector at higher speeds. This is shown in Figure IV.15, which shows the detector

Table IV.5: N-Well/P-substrate photodetector rise time vs. reverse bias, at 200 MHz

V_{bias}	10% -- 90% t_{rise}
0.0 V	2.3 $nsec$
1.0 V	2.1 $nsec$
3.0 V	1.8 $nsec$

response to long strings of 1s and 0s, with short bursts of 2.5 $nsec$ pulses in between. It is clearly difficult to set a fixed threshold between 1 and 0 in this case, as it is signal dependent.

IV.D.2 PRBS results

Figures IV.16 and IV.17 show the results of the optical tests using PRBS data with receivers R10 and R8 respectively. The optical power for receiver R10 was 40 μW, and the bit-rate was 100 Mb/s. For receiver R8 it was 240 μW at 200 Mb/s. The average optical power was higher than predicted by the electrical measurements because of the non-zero extinction ratio of the optical source, the lower responsivity of the actual detector as compared to the model, and the base-line wander due to the slowly diffusing carriers. The effect of the base-line wander is to increase the jitter when long strings of 1s and 0s are encountered in the data. This is seen in the eye-diagrams by the large transition regions with no sharply defined edge. The limiting component in the link is clearly the detector, since the electrical tests show that the receivers are capable of operating more than 5 times faster than measured optically.

IV.E Coding for CMOS detectors

One way to reduce the base-line wander is to code the data so that the average energy per symbol is the same. This way, the slow component of the photocurrent is the same for every symbol, and becomes a constant average value

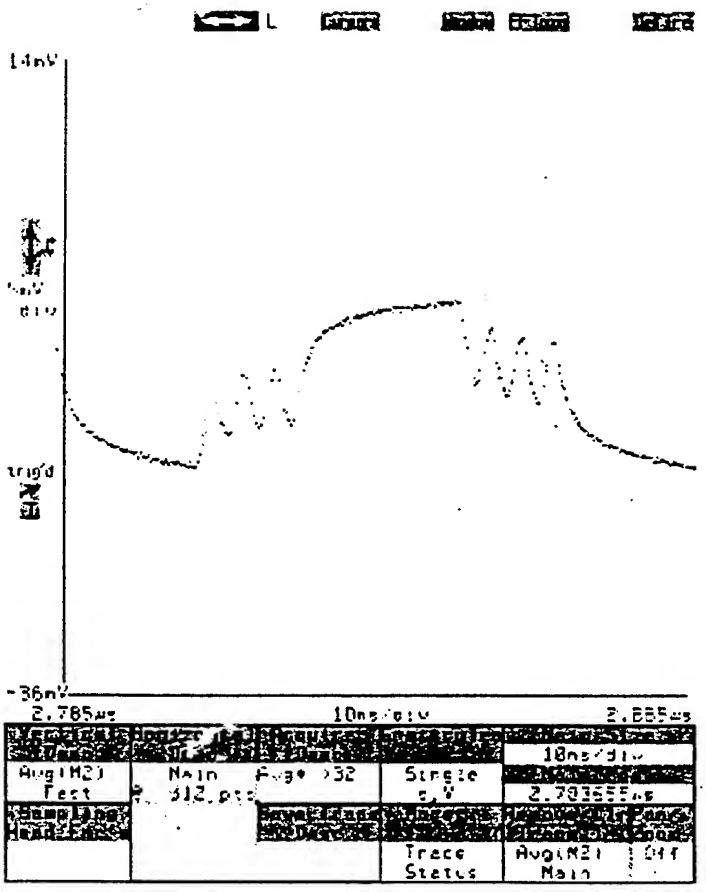


Figure IV.15: Base-line wander in the N-Well/P-substrate detector due to the long diffusion time of carriers.

Figure IV.16: Eye diagram of optical tests with PRBS on receiver R10. The bit-rate was 100 Mb/s and the average optical power was 40 μW.

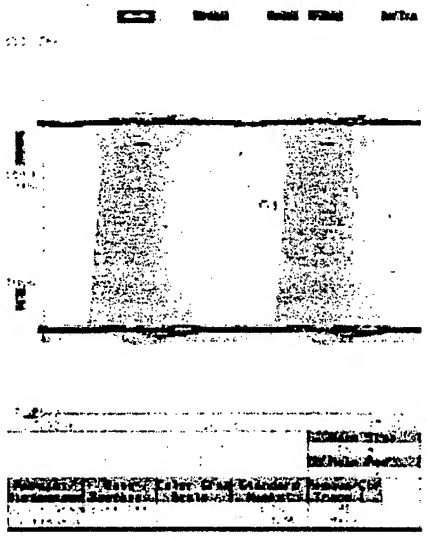


Figure IV.17: Eye diagram of optical tests with PRBS on receiver R8. The bit-rate was 200 Mb/s and the average optical power was 240 μW.

Table IV.6: Binary (manchester coded) vs. Ternary PPM

Code	Binary	Binary PPM	Ternary PPM
1	0 0 0	01 01 01	001 001
2	0 0 1	01 01 10	001 010
3	0 1 0	01 10 01	001 100
4	0 1 1	01 10 10	010 001
5	1 0 0	10 01 01	010 010
6	1 0 1	10 01 10	010 100
7	1 1 0	10 10 01	100 001
8	1 1 1	10 10 10	100 010
9			100 100

that is not signal dependent. Such a general code is pulse-position modulation (PPM). PPM is a coding scheme where the position of the pulse in the symbol determines the symbol value. PPM has been shown to be a well-suited code for low power optical systems. [70] If the PPM alphabet size is given by Q, then binary ($Q = 2$) PPM is manchester (time differential) coding.

The rate of information transfer is given by r, with units *nats/sec.* The amount of information per pulse-slot for PPM is given by

$$rT_s = \frac{ln(Q)}{Q} \leq \frac{ln(3)}{3} \tag{IV.2}$$

where the units are *nats/slot.* Here, T_s is the pulse-slot size in seconds. The inequality indicates that ternary PPM ($Q = 3$) yields the largest information throughput for a fixed pulse-slot size.

The advantage of ternary PPM can be seen from Table IV.6. Here, in six bits (or pulse-slots), only 8 codes are possible with binary PPM, whereas 9 codes are possible with ternary PPM. Ternary PPM reduces the average optical power compared to binary PPM, while keeping the energy per symbol constant to eliminate base-line wander.

It would be possible to use all 9 symbols for information transfer. Unfortunately, transforming the 9 symbols into a binary value for computation is non-trivial. A better use for the extra symbol would be to maintain code synchro-

nization by mixing in the extra symbol to break up long strings of the same code. For example, a long string of the codes "..0 010 010 010 010 010 010" could be mis-interpreted as "001 001 001 001 001 001 0.." if the synchronization with the first code pulse-slot is lost. If the extra code is used whenever this symbol repeats, then this string becomes "..0 010 010 *001 100* 010 010" (assuming the extra code is "001 100"), and the synchronization will be recovered. The code "001 100" is a good choice for re-synchronization because there is only one choice for the first code pulse-slot that leads to a valid ternary PPM code.

Figures IV.18 and IV.19 are eye-diagrams of the optical tests of receivers R10 and R8 using a ternary PPM data stream. The ternary PPM data stream is generated by the pulse-generator with the programmed sequence "001 010 001 100 100 010 001 100 100 010 10" where the last two bits were required to fill the 32-bit data pattern used by the pulse generator. Although this is not a random sequence, the sequence was chosen to cover as many pulse-slot spacings as possible.

The pulse-slot rate for the R10 receiver was 400 $Mslot/s$, which translates to a bit-rate of 200 $Mbit/s$. The R8 receiver operated at 300 $Mbit/s$. The eye-diagrams are more open and sharply defined than in the uncoded PRBS case, and the effective data rate is higher even though coding is being used. This clearly demonstrates the value of coding the data stream when using the N-Well/P-substrate CMOS detector.

IV.F Conclusion

In conclusion, the test results from the fabricated receiver test-chip validated the receiver model and optimization presented in appendix III. Receivers designed for less than 1 $Gbit/s$ operation had characteristics very close to those predicted by the model. Operation above 1.1 $Gbit/s$ was most likely limited by the off-chip driver on the test-chip.

A CMOS compatible detector was also tested and characterized together

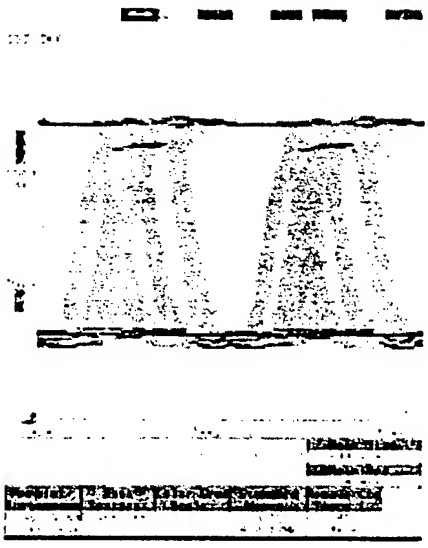


Figure IV.18: Eye diagram of optical tests with ternary PPM on receiver R10. The pulse-slot rate was 400 $Mslot/s$. The average optical power was 40 μW.

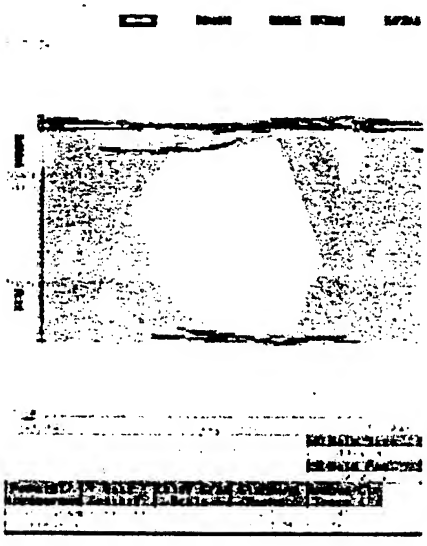


Figure IV.19: Eye diagram of optical tests with ternary PPM on receiver R8. The pulse-slot rate was 600 $Mslot/s$. The average optical power was 240 μW.

with the optimized receivers. Operation at low data rates ($< 200 Mbit/s$) was demonstrated with uncoded data. A data coding algorithm was suggested to compensate for the long diffusion time of carriers in CMOS-compatible detectors. The improvements when using this data coding were verified experimentally, allowing the data rate to increase to 300 $Mbit/s$.

Appendix V

V. GAIN-BANDWIDTH PRODUCT OF A VCSEL AMPLIFIER

V.1. Introduction

The first condition that a VCSEL amplifier needs to satisfy is that it should be able to provide high gain without limiting the system bit rate, or equivalently, it has to demonstrate a high gain-bandwidth product. In the following, we use an equivalent electrical circuit to model the VCSEL amplifier, and we derive an analytical expression for its gain-bandwidth product. We then verify this theoretical expression with experimental data and propose an optimum structure for a VCSEL amplifier.

The small signal behavior of a semiconductor laser is modeled with equivalent passive electrical circuits where electrical modulation, optical modulation (i.e. laser as an optical amplifier), and multimode operation of the laser are accounted for. These circuits offer a fast and efficient simulation tool with very little computational complexity, where the small-signal assumption (i.e. small modulation range) is not violated or is sufficient enough for the simulation.

Then, the equivalent circuit for the case of optical modulation is used to derive an analytical expression for the gain-bandwidth product of a VCSEL amplifier. Experimental results for the steady-state gain and the -3dB bandwidth of the optical amplifier are used to verify the theory, which predicts gain-bandwidth products of 111 GHz and 556 GHz for VCSELs with three 85Å-thick quantum wells with optical gains of 1000 cm^{-1} and 5000 cm^{-1}, respectively. Small-signal steady-state gains of over 23 dB are demonstrated. The effects of saturation and biasing conditions are also studied and measured. It is shown that biasing the VCSEL at its threshold provides the maximum steady-state gain, and the maximum gain-bandwidth product. The maximum gain-bandwidth product is directly proportional to the photon loss rate from the output mirror (α_m). To maximize it, the reflectivity of both mirrors must be lowered (~ 97%) and optimized to a value where the optical gain is barely sufficient to compensate the total mirror loss (i.e. where threshold can barely be reached). The proposed VCSEL amplifier structure can also be used as an ultra low voltage (~ 50 mV), high contrast ratio (> 10:1), high speed (> 1 GHz) optical light modulator.

Semiconductor lasers have been extensively modeled in terms of equivalent electrical circuits [1,2,3,4,5] to simulate their large-signal behavior. However, since the laser behavior includes nonlinear effects, accurate models tend to be computationally very demanding. For simulations, where speed is favored over accuracy or where the operation of the laser is limited to a small modulation range, it is more advantageous to model the small-signal behavior of the laser. In this case, the laser equations are reduced to linear differential equations, and the electrical circuits that model the laser are significantly simplified. Previously, based on the impedance characteristics of a laser [6], an equivalent electrical circuit has been proposed to model the small-signal behavior of lasers in the presence of small perturbations [7]. This circuit has been further modified to include the effects of lateral carrier diffusion [8] and of package parasitics [9] under electrical modulation.

In section V.2, we exploit the similarities between semiconductor lasers and electrical RLC circuits to repeat the derivations of the above electrical circuits, which exactly model the small-signal behavior of semiconductor lasers under electrical modulation. We then extend our derivations to include optical modulation (i.e. when a laser is used as an optical amplifier) and multi-mode lasers, where the secondary modes can be longitudinal, spatial, and/or polarization modes. In Section V.2.1, we state the small-signal rate equations, and outline the procedure to convert these equations into current and voltage equations of RLC circuits. This procedure is then applied to electrical modulation (section V.2.2), and the resulting circuit is compared with the previously published circuits for verification of our model. In Sections V.2.3 and V.2.4, we modify the equations and our electrical circuit to include optical modulation as well as multi-mode operation of a laser.

The next section (Section V.3) investigates the performance of a VCSEL amplifier in terms of its gain-bandwidth product. Semiconductor laser amplifiers (SLA's) have been used for amplification of an external optical signal beam in optical and optoelectronic communication systems [10,11,12,13], and their gain and noise characteristics have been previously studied [3,4,14,15]. In a free space optoelectronic interconnection system, optical amplifiers can be employed to either reduce the gain required from the receiver circuits, or to reduce the optical power required from the transmitters. Both cases decrease the power dissipation in the receivers and the transmitters, and increase the bandwidth and the interconnect density of the system [16,17]. In these applications, SLAs are advantageous over electronic amplifiers (e.g. avalanche photo-diodes) due to their high bandwidths, and their low supply voltages, which enable them to be integrated with electronic circuits.

For free space optically interconnected systems, VCSEL amplifiers can offer certain critical advantages over edge-emitting SLAs. These advantages include higher GBW product, very high packing density due to 2-dimensional array fabrication, low coupling losses due to circular cavity geometry, and low noise due to single mode operation (i.e. no mode-partitioning noise). The feasibility of VCSEL amplifiers has been studied theoretically [18,19,20] and demonstrated experimentally [21,22,23,24,25].

In section V.3, we use an equivalent electrical circuit to derive the small-signal steady-state gain, and -3dB bandwidth of a VCSEL amplifier under different biasing conditions. We then combine the two results to obtain a simple theoretical expression for the maximum gain-bandwidth product of the amplifier, and we report experimental results to verify the theoretical predictions and expressions. Then, we discuss the practical system issues in using a VCSEL as an amplifier, and finally, we show that the proposed VCSEL amplifier structure can also be used as an ultra low voltage (~ 50 mV), high contrast ratio (> 10:1), high speed (> 1 GHz) optical light modulator.

In Section V.3.1, to derive analytical expressions for the gain, bandwidth, and the maximum gain-bandwidth product of VCSEL amplifiers, we utilize a passive electronic circuit, whose voltage and current equations are exactly equivalent to the small-signal rate equations of a semiconductor laser under external optical modulation (derived in section V.2.3). Section V.3.2 presents the experimental data that validates

the theory of section V.3.1. Section V.3.3 proposes an optimal VCSEL amplifier structure and the expected GBW product for typical device parameters, and discusses the system issues to make the device practical. Section V.3.4 outlines the method to use the VCSEL amplifier structure as an efficient optical light modulator. Section V.6 concludes the paper.

V.2. Small Signal Equivalent Circuits for a Semiconductor Laser

V.2.1. Analogies between semiconductor lasers and RLC circuits

Rate equations can be utilized for a simple treatment of the frequency and/or time-domain behaviors of the electron and photon numbers in a laser cavity. The reader is referred to any textbook on lasers for a discussion of the rate equations, and their validity for various laser phenomena (e.g. [26]). The general rate equations for a single mode laser are

$$\dot{P}(t) = G \cdot P(t) - \gamma \cdot P(t) + R_{sp}$$

$$\dot{N}(t) = \frac{I_{bias}}{q} - \gamma_e \cdot N(t) - G \cdot P(t)$$

Equation V.1(a,b)

where P and N are the total number of photons in the lasing mode and electrons in the excited state inside the cavity, respectively. The dots on top of P and N represent time derivatives. The three terms on the right hand side of the first equation are, in order, the stimulated emission rate, the total photon loss rate including the loss through the mirrors, and the spontaneous emission rate into the lasing mode. The three terms in the second equation are, in order, the injection rate of electrons into the gain medium, the electron loss rate (including nonradiative recombination, spontaneous emission and Auger recombination), and the loss rate of electrons due to stimulated emission.

To derive the linearized small-signal rate equations of a single mode laser, the total photon number in the lasing mode (P) and the electron number in the excited state (N) inside the cavity in Equation V.1(a,b) are replaced by P + δP and N + δN, respectively. δP and δN are perturbations to the steady-state values, and are functions of time. The total photon loss rate (γ) is assumed to stay constant, whereas the stimulated emission gain (G), the spontaneous emission rate into the lasing mode (R_{sp}), and the total electron loss rate (γ_e) (excluding the loss due to stimulated emission) are expanded in truncated Taylor series as follows:

$$G(N,P) \cong G + \frac{\partial G}{\partial N} \cdot \delta N + \frac{\partial G}{\partial P} \cdot \delta P$$

$$R_{sp}(N,P) \cong R_{sp} + \frac{\partial R_{sp}}{\partial N} \cdot \delta N$$

$$\gamma_e(N,P) \cong \gamma_e + \frac{\partial \gamma_e}{\partial N} \cdot \delta N$$

Equation V.2(a,b,c)

Substituting Equation V.2(a,b,c) into Equation V.1(a,b), subtracting Equation V.1(a,b) from the resulting expressions, substituting $(-R_{sp}/P)$ for $(G-\gamma)$ (from the steady-state solution of Equation V.1(a)), and ignoring all the second order terms in δP and/or δN, we get the linearized small-signal rate equations in the presence of a small perturbation (i.e. assuming $\delta P << P$ and $\delta N << N$) [26]

$$\delta P(t) = -\Gamma_P \cdot \delta P(t) + \sigma_{N\to P} \cdot \delta N(t)$$

$$\delta N(t) = -\Gamma_N \cdot \delta N(t) - \sigma_{P\to N} \cdot \delta P(t)$$

Equation V.3(a,b)

where Γ_P and Γ_N are the decay rates of fluctuations of the photon and electron numbers, respectively, and $\sigma_{N->P}$ and $\sigma_{P->N}$ are the coupling coefficients between the photon and the electron number fluctuations. Note that the electron and the photon numbers in Equation V.3(a,b) (δN and δP) refer to the deviations from the equilibrium values at a given bias of the laser. At a given bias point, which fixes P and N, the four coefficients in Equation V.3(a,b) are given as

$$\Gamma_P = \frac{R_{sp}}{P} - G_P \cdot P \quad ; \quad \Gamma_N = \gamma_e + \gamma_{e_N} \cdot N + G_N \cdot P$$

$$\sigma_{N\to P} = G_N \cdot P + R_{sp_N} \quad ; \quad \sigma_{P\to N} = G + G_P \cdot P$$

Equation V.4(a,b,c,d)

where the subscript of P or N on the right side of the equations mean the derivatives with respect to P or N, respectively.

At this point, we note that the small-signal rate equations are two linearly coupled differential equations, similar to the voltage and current equations of an RLC circuit. In a laser cavity, the electrons and the photons exchange energy through absorption and emission with the various loss mechanisms dissipating energy in the cavity. Similarly, in an RLC circuit, the capacitor and the inductor exchange energy, and the resistor dissipates energy out of the circuit. In addition, the continuity conditions of the electrical circuit (i.e. voltage across the capacitor and current across the inductor are continuous) are equivalent to those of the laser cavity (i.e. the changes in the electron and photon numbers inside the cavity are continuous if rate equations are being utilized). Motivated by these analogies, we make the assumption that the excited electrons in a laser cavity can be represented with the charge across a

capacitor, and the photons in a given mode of the laser with the magnetic flux linkage of an inductor

$$\delta P(t) = \frac{\Psi(t)}{q \cdot (\text{Henry/sec})} \quad ; \quad \delta N(t) = \frac{Q(t)}{q}$$

Equation V.5(a,b)

where division by the electronic charge (q) and by the fixed units of (Henry / sec) are to ensure proper units for the components in the electrical circuit. Assigning electrons to an inductor and photons to a capacitor still would have given us the same results, but the component values in the electrical circuits would turn out to be negative.

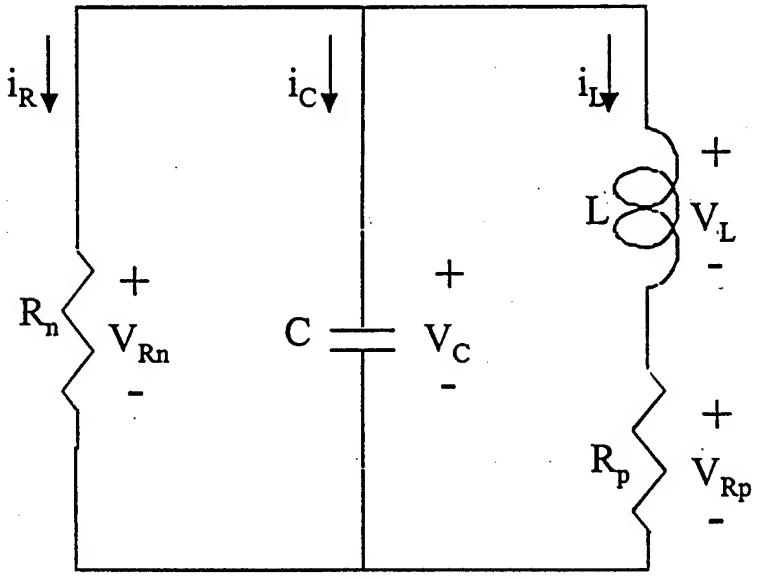
We use Equation V.5(a,b) and the standard equations for a capacitor and an inductor (i.e. $Q = C\,V_C$, $i_C = dQ / dt$; $\Psi = L\,i_L$, $V_L = d\Psi / dt$) to convert Equation V.3(a,b) into voltage and current equations

$$v_L(t) = -\Gamma_P \cdot L \cdot i_L(t) + \sigma_{N\to P} \cdot C \cdot v_C(t) \cdot (H/s)$$

$$i_C(t) = -\Gamma_N \cdot C \cdot v_C(t) - \frac{\sigma_{P\to N} \cdot L \cdot i_L(t)}{(H/s)}$$

Equation V.6(a,b)

Equation V.6(a,b) are the voltage and current equations of the circuit given in Figure V.1 (with a proper choice of component values). This circuit is exactly the same as the one given in [7] to model the small-signal behavior of a single mode laser in the presence of small perturbation.



$$\delta P(t) = \frac{L\,i_L(t)}{q\ (\text{Henry/sec})}$$

$$\delta N(t) = \frac{C\,v_C(t)}{q}$$

$$L = \frac{(H/s)}{\sigma_{P\to N}}$$

$$C = \frac{1}{(H/s)\ \sigma_{N\to P}}$$

$$R_n = \frac{(H/s)\ \sigma_{N\to P}}{\Gamma_N}$$

$$R_p = \frac{(H/s)\ \Gamma_P}{\sigma_{P\to N}}$$

Figure V.1 Small signal circuit model of a single mode laser in the presence of small perturbation.

The output light power of the laser ($\delta P_{out}(t)$) is the product of the deviation of the photon number from the equilibrium value ($\delta P(t)$), the unit photon energy ($h\nu$), and the photon loss rate through the output mirror (α_m), so from Equation V.5(a) and Figure V.1, we have

$$\delta P_{out}(t) = \alpha_m \cdot \frac{L \cdot i_L(t)}{q \cdot (H/s)} \cdot h\nu$$

Equation V.7

V.2.2. Electrical Modulation

For an arbitrary external electrical modulation ($i_m(t)$), Equation V.3(b) is modified

$$\delta N(t) = -\Gamma_N \cdot \delta N(t) - \sigma_{P\to N} \cdot \delta P(t) + \frac{i_m(t)}{q}$$

Equation V.8

such that the current equation of Equation V.6(b) becomes

$$i_C(t) = -\Gamma_C \cdot C \cdot v_C(t) - \frac{\sigma_{P\to N} \cdot L \cdot i_L(t)}{(H/s)} + i_m(t)$$

Equation V.9

The circuit is then modified as in Figure V.2, and including the electrical parasitics associated with an external current source gives us the circuit published in [9].

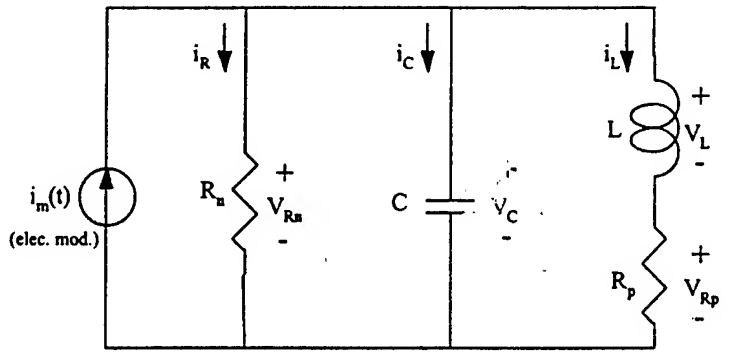


Figure V.2 Small signal circuit model of a single mode laser with electrical modulation.

V.2.3. Optical modulation

By choosing an appropriate bias point, a laser can be operated as an optical amplifier [10,11,12,13]. In this case, the photon number for a given laser mode is externally modulated, so Equation V.1(a) is changed to read

$$\dot{P}(t) = G \cdot P(t) - \gamma \cdot P(t) + R_{sp} + \eta_c \cdot \frac{P_{in}(t)}{h\nu}$$

Equation V.10

where $P_{in}(t)$ is the input light power. As a result, Equation V.3(a) is modified as

$$\delta\dot{P}(t) = -\Gamma_P \cdot \delta P(t) + \sigma_{N\to P} \cdot \delta N(t) + \eta_c \cdot \frac{P_{in}(t)}{h\nu}$$

Equation V.11

and in return, the voltage equation of Equation V.6(a) becomes

$$v_L(t) = -\Gamma_P \cdot L \cdot i_L(t) + \sigma_{N\to P} \cdot C \cdot v_C(t) \cdot (H/s) + \frac{q \cdot (H/s) \cdot \eta_c \cdot P_{in}(t)}{h\nu}$$

Equation V.12

where η_c is the coupling efficiency of the optical input signal into the Fabry-Perot cavity of the laser

$$\eta_c = \frac{T_1(1-R_2)}{1 + R_1R_2 - 2\sqrt{R_1R_2}\cos\delta}$$

Equation V.13

In Equation V.13, subscripts 1 and 2 refer to the input mirror and the second mirror, respectively. T and R are the transmittance and the reflectance of each mirror, and the absorption in the mirrors (i.e. T+R+A=1) as well as unequal mirror reflectivity (i.e. R1 R2) are taken into account: δ is the mismatch between the wavelength of the input signal and the optical round-trip path length of the cavity. The above equation is obtained by slightly modifying the procedure given in [27], where the transmittance of a passive Fabry-Perot interferometer is calculated.

The additional term in Equation V.12 adds to the voltage across the inductor, so it is equivalent to placing a voltage source in series with the inductor-resistor pair in the equivalent electrical circuit (Figure V.3).

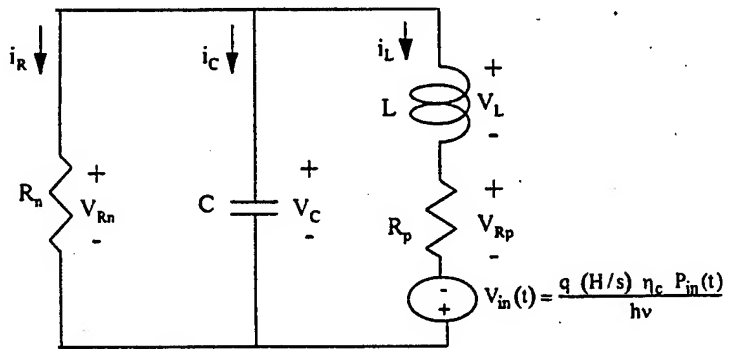


Figure V.3 Small signal circuit of a single mode laser under optical modulation.

V.2.4. Multi-mode lasers

The model for a multi-mode laser is more involved. When more than one mode exists in the laser, the rate equations of Equation V.1(a,b) become

$$\dot{P}_k(t) = G_k \cdot P_k(t) - \gamma_k \cdot P_k(t) + R_{sp_k}$$

$$\dot{N}(t) = \frac{I_{bias}}{q} - \gamma_e \cdot N(t) - \sum_k G_k \cdot P_k(t)$$

Equation V.14(a,b)

where k is the mode number (i.e. Equation V.14(a) is actually a set of k equations for k modes). Following the same procedure as in the single mode laser, the small-signal rate equations (analogous to Equation V.3(a,b)) are derived

$$\delta\dot{P}_1(t) = -\Gamma_{P_1} \cdot \delta P_1(t) + \sigma_{N\to P_1} \cdot \delta N(t)$$

$$\vdots$$

$$\delta\dot{P}_k(t) = -\Gamma_{P_k} \cdot \delta P_k(t) + \sigma_{N\to P_k} \cdot \delta N(t)$$

$$\delta\dot{N}(t) = -\Gamma_N \cdot \delta N(t) - \sum_k \sigma_{P_k\to N} \cdot \delta P_k(t)$$

Equation V.15(a_1,...,a_k,b)

where the expressions for the decay rates and the coupling coefficients (i.e. Equation V.4(a,b,c,d)) are now given separately for each mode by simply adding a subscript from 1 to k to each of the P terms.

Using Equation V.5(a,b), along with the standard current-voltage equations for a capacitor and an inductor, in Equation V.15(a1,...,ak,b), and rearranging the q and (H / s) terms, we obtain one current equation and k voltage equations (one for each of the k modes)

$$v_{L_1}(t) = -\Gamma_{P_1} \cdot L_1 \cdot i_{L_1}(t) + \sigma_{N\to P_1} \cdot C \cdot v_C(t) \cdot (H/s)$$

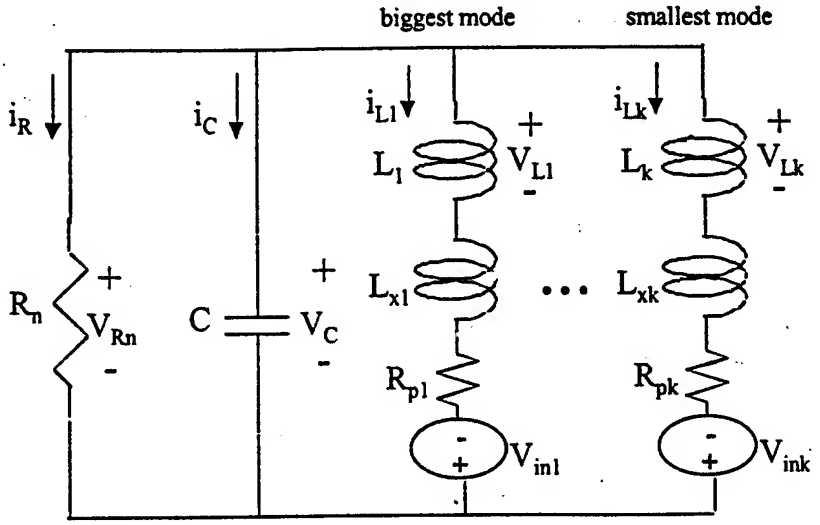
$$\vdots$$

$$v_{L_k}(t) = -\Gamma_{P_k} \cdot L_k \cdot i_{L_k}(t) + \sigma_{N\to P_k} \cdot C \cdot v_C(t) \cdot (H/s)$$

$$i_C(t) = -\Gamma_N \cdot C \cdot v_C(t) - \sum_k \frac{\sigma_{P_k\to N} \cdot L_k \cdot i_{L_k}(t)}{(H/s)}$$

Equation V.16

The circuit satisfying all of the above equations is not a trivial one, and the resulting circuit is given in Figure V.4, along with the component values.



$$R_n = \frac{(H/s)\,\sigma_{N\to P_1}}{\Gamma_N} \quad ; \quad C = \frac{1}{(H/s)\,\sigma_{N\to P_1}}$$

$$L_j = \frac{(H/s)}{\sigma_{P_j\to N}} \quad ; \quad L_{xj} = L_j\left(\frac{\sigma_{N\to P_1}}{\sigma_{N\to P_j}} - 1\right) \quad (j = 1,\ldots,k)$$

$$R_{Pj} = \frac{(H/s)\,\Gamma_{Pj}}{\sigma_{P_j\to N}}\,\frac{\sigma_{N\to P_1}}{\sigma_{N\to P_j}} \quad ; \quad V_{inj}(t) = \frac{q\,(H/s)\,\eta_c\,P_{inj}(t)}{h\nu}\,\frac{\sigma_{N\to P_1}}{\sigma_{N\to P_j}}$$

Figure V.4 Small signal circuit model of a multimode laser.

Note that each inductor (L_j), which represents an optical mode, is now accompanied by a second inductor (L_{xj}) to account for the reduction in the coupling coefficient of that mode with the electrons. The output power of each mode is proportional to only L_j, and not L_{xj}. The dominant mode is expressed by the leftmost inductor-resistor pair (i.e. mode 1 in Figure V.4). This mode has the highest coupling with the electrons, so it has the smallest R_{pj}, L_j, and L_{xj}. The addition of external modulation to the circuit is exactly the same as explained in Sections V.2.2 and V.2.3. A current source in parallel with R_n is added to account for electrical modulation, and a voltage source is added in series with an inductor-resistor pair, whose mode matches that of the optical input signal (shown in Figure V.4).

V.3. Theory and Experiment for the Gain-Bandwidth Product of a VCSEL Amplifier

V.3.1. Theory

V.3.1.1. Analytical expression for GBW product

The simplest set of equations to study the interaction between the electrons and the photons in a semiconductor cavity are the rate equations. The general rate equations for a single mode laser are given in Equation V.1(a,b), and repeated below for convenience

$$\dot{P}(t) = G \cdot P(t) - \gamma \cdot P(t) + R_{sp}$$

$$\dot{N}(t) = \frac{I_{bias}}{q} - \gamma_e \cdot N(t) - G \cdot P(t)$$

Equation V.17(a,b)

At a given bias point (i.e. for a fixed I_{bias}, P, and N), if we assume a small perturbation to the electron and photon numbers such that $\delta P \ll P$ and $\delta N \ll N$, Equation V.17(a,b) can be converted to linearized small-signal rate equations (given in Equation V.11 and Equation V.3(b)):

$$\delta\dot{P}(t) = -\Gamma_P \cdot \delta P(t) + \sigma_{N\to P} \cdot \delta N(t) + \eta_c \cdot \frac{P_{in}(t)}{h\nu}$$

$$\delta\dot{N}(t) = -\Gamma_N \cdot \delta N(t) - \sigma_{P\to N} \cdot \delta P(t)$$

Equation V.18(a,b)

where we have included the last term in Equation V.18(a) to account for the optical input power (P_{in}). η_c is the coupling efficiency of the input beam into the Fabry-Perot cavity and is given in Equation V.13.

A passive equivalent electronic circuit has been proposed to model a single mode semiconductor laser under external optical modulation (Section V.2.3),[28]. The voltage and current equations of this electronic circuit are exactly equivalent to the linearized small signal rate equations of a laser (i.e.Equation V.18(a,b)) with a proper choice of component values for the circuit (Figure V.3). The perturbations to the electron number ($\delta N(t)$) and to the photon number ($\delta P(t)$) inside the cavity are equal to the charge across the capacitor and the magnetic flux linkage of the inductor, respectively. The output light power ($P_{out}(t)$) is the product of the inductor's magnetic flux linkage ($L\, i_L(t) = \delta P(t)$) and the photon loss rate from the output mirror (α_m):

$$P_{out}(t) = \alpha_m \cdot \delta P(t) = \alpha_m \cdot L \cdot i_L(t)$$

Equation V.19

$$\text{and } \alpha_m = T_m \cdot \frac{c}{2l_{cavity,eff.}}$$

Equation V.20

where 'm' is the subscript for the output mirror, T is the mirror transmission, and $l_{cavity,eff.}$ is the effective cavity length including the penetration of the field into the mirrors.

To find the gain and the bandwidth of the amplifier, we apply a sinusoidal input: $P_{in}(t) = P_{in} \sin(\omega_m t)$ to the circuit of Figure V.3. Using Equation V.19, we get the gain of the amplifier as a function of modulation frequency:

$$\text{Gain}(\omega_m) = \frac{P_{out}(\omega_m)}{P_{in}(\omega_m)} = \frac{\eta_c \alpha_m L i_L}{V_{in}} = \frac{\eta_c \alpha_m L}{\left[\left(\frac{R_n}{1 + i\omega_m R_n C}\right) + i\omega_m L + R_p\right]}$$

Equation V.21

which can be arranged in a more intuitive way to show the interaction between the frequency pole due to the optical mode at ($R_p/L = \Gamma_p$) and the pole due to the electrons at ($1/R_nC = \Gamma_n$):

$$\text{Gain}(\omega_m) = \frac{\eta_c \alpha_m (\Gamma_n + i\omega_m)}{(\Gamma_n + i\omega_m)\cdot(\Gamma_p + i\omega_m) + (\sigma_{N\to P} \cdot \sigma_{P\to N})}$$

Equation V.22

Taking the absolute value of the expression, we get:

$$|\text{Gain}(\omega_m)| = \frac{\eta_c \alpha_m (\Gamma_n^2 + \omega_m^2)^{\frac{1}{2}}}{\left[(\sigma_{N\to P} \cdot \sigma_{P\to N} + \Gamma_n \cdot \Gamma_p - \omega_m^2)^2 + (\Gamma_n + \Gamma_p)^2 \cdot \omega_m^2\right]^{\frac{1}{2}}}$$

Equation V.23

If a semiconductor laser is biased above its threshold, its transient behavior in response to a perturbation is expressed with two parameters: the damping rate (Γ_R) and the relaxation oscillation frequency (Ω_R). These are given as [26]:

$$\Gamma_R = \frac{1}{2}(\Gamma_n + \Gamma_p)$$

$$\Omega_R = \sqrt{\sigma_{N\to P} \cdot \sigma_{P\to N} - \frac{1}{4}(\Gamma_n - \Gamma_p)^2}$$

$$\Gamma_X = \sqrt{-\Omega_R^2} = \sqrt{\frac{1}{4}(\Gamma_n - \Gamma_p)^2 - \sigma_{N\to P} \cdot \sigma_{P\to N}}$$

Equation V.24(a,b,c)

By definition, at the threshold of the laser, $\Omega_R = 0$. If biased below threshold, the expression under the square root in Equation V.24(b) becomes negative, so in Equation V.24(c), we defined a third parameter (Γ_X) for the case of a laser biased below threshold.

Substituting the parameters from Equation V.24 into Equation V.23, we get the gain of the amplifier for the two different biasing conditions, below and above threshold:

$$\text{Gain}(\omega_m) = \frac{\eta_c \alpha_m \left(\Gamma_n^2 + \omega_m^2\right)^{\frac{1}{2}}}{\left[\left(\Gamma_R^2 - \Gamma_X^2 - \omega_m^2\right)^2 + 4\Gamma_R^2 \omega_m^2\right]^{\frac{1}{2}}} \quad \text{for } I_{bias} < I_{th}$$

$$\text{Gain}(\omega_m) = \frac{\eta_c \alpha_m \left(\Gamma_n^2 + \omega_m^2\right)^{\frac{1}{2}}}{\left[\left(\Gamma_R^2 + \Omega_R^2 - \omega_m^2\right)^2 + 4\Gamma_R^2 \omega_m^2\right]^{\frac{1}{2}}} \quad \text{for } I_{bias} > I_{th}$$

Equation V.25(a,b)

The former case corresponds to an overdamped circuit in Figure V.3, where the equilibrium point is reached through an exponential decay. The latter case, in turn, corresponds to an underdamped circuit, which experiences damped oscillations before reaching equilibrium (i.e. relaxation oscillations in a laser).

To find the steady-state gain, we set $\omega_m = 0$, and both Equation V.25(a,b) converge at the same maximum gain when the amplifier is biased exactly at threshold (i.e. $\Omega_R = \Gamma_X = 0$):

$$\text{Gain}_{\text{steady-state,max imum}} = \frac{\eta_c \alpha_m \Gamma_n}{\Gamma_R^2} \quad \text{for } I_{bias} = I_{th}$$

Equation V.26

The fact that maximum gain is achieved at threshold can be qualitatively explained as follows: the gain depends on the number of electrons available inside the cavity for stimulated emission such that when the input photons enter the cavity, they will use this reservoir of electrons for amplification. Below threshold, increasing the bias current up to the threshold current continuously increases the electron number in the cavity, and thus the gain. On the other hand, above threshold, the electron number in the cavity is approximately clamped at the threshold value, but increasing the bias current any further increases the number of photons in the cavity. These photons compete with the input signal photons, such that the number of electrons available for amplification 'per photon' has declined. As a result, the gain of the amplifier drops with an increase in the bias current above threshold.

For a VCSEL biased at threshold, we set $\Omega_R = 0$ in Equation V.25(b), and we solve for the -3dB bandwidth of the amplifier (i.e. ω_m at which the gain drops to 1/2 of

its steady state value). If we let $\Gamma_n = y\,\Gamma_R$ at threshold, where (y) is a constant, we have:

$$f_{-3dB} = \frac{\omega_{-3dB}}{2\pi} = \frac{\Gamma_R}{2\pi}\cdot\left[\left(\frac{2}{y^2}-1\right)+2\left(1-\frac{1}{y^2}+\frac{1}{y^4}\right)^{\frac{1}{2}}\right]^{\frac{1}{2}}$$

Equation V.27

If the bias current is moved away from threshold, both the steady-state gain and the bandwidth of the amplifier decrease. Furthermore, the expression for bandwidth is no longer a simple one, and the exact bandwidth of the device can only be computed numerically from Equation V.25(a,b).

Making the same substitution of $\Gamma_n = y\,\Gamma_R$ in Equation V.26, and multiplying Equation V.26 with Equation V.27, we get the maximum gain-bandwidth product of the amplifier, which occurs when it is biased at its threshold:

$$GBW_{max\,imum} = \frac{\eta_c\cdot\alpha_m}{2\pi}\cdot\left\{y\cdot\left[\left(\frac{2}{y^2}-1\right)+2\left(1-\frac{1}{y^2}+\frac{1}{y^4}\right)^{\frac{1}{2}}\right]^{\frac{1}{2}}\right\}$$

Equation V.28

From Equation V.24(a), as the ratio of Γ_n and Γ_p changes from $\Gamma_n << \Gamma_p$ to $\Gamma_n >> \Gamma_p$, the constant (y) goes from 0 to 2. Within this range, the expression in curly brackets in Equation V.28 lies between 1.73 and 2.23 (plotted in Figure V.5), so we can approximate the whole expression to 2 to get a simple equation for the maximum gain-bandwidth product independent of (y):

$$GBW_{max\,imum} \cong \frac{\eta_c\cdot\alpha_m}{\pi}$$

Equation V.29

Equation V.29 is valid for a semiconductor amplifier, where it is assumed that the device is single mode, and that it is biased at the threshold of that optical mode. These two conditions imply that for a given input beam with a certain longitudinal frequency, spatial profile and polarization, the device is biased at the point where the cavity mode that matches the input beam in all three characteristics is at its threshold. This bias point is not necessarily equal to the device threshold because as the bias current is increased to above the device threshold, the laser may experience mode hopping to different spatial or polarization modes. In this case, if the input beam matches any one of these new modes, the mode threshold will be the bias current where that mode becomes the dominant mode, and not when the device starts lasing. The two assumptions (i.e. single-mode operation and biasing at threshold) also imply that at that bias point, there is no other cavity mode at or close to its threshold.

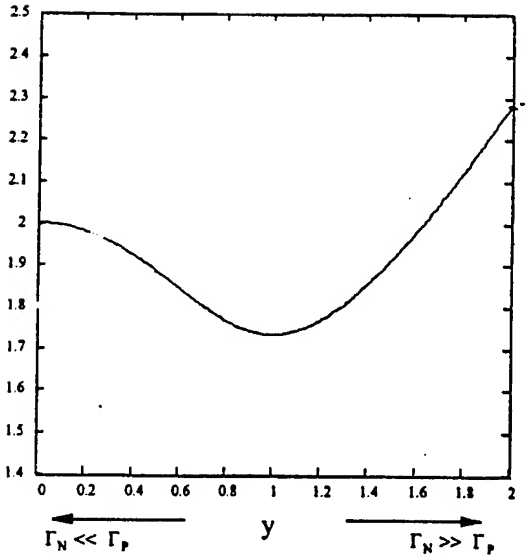


Figure V.5 Value of expression in 'y' as Γ_N goes from << Γ_P to >> Γ_P.

In practice, small diameter VCSELs (i.e. diameter < ~6μm) have only one spatial mode. Also by introducing an asymmetry either to the shape of the cavity or to the gain and/or loss mechanisms inside the cavity, the device can be forced to operate in a specific polarization. This ensures single mode operation. However, decreasing the diameter of the device decreases the alignment tolerance of the system optics, so for amplification, midsize VCSEL structures (i.e. 10-25 μm) may be preferred. In this case, multiple modes can co-exist at a given bias point, and the previous assumption of single mode operation to obtain Equation V.29 may be violated.

For the case of an amplifier where two cavity modes have the same threshold, the small signal rate equations in Equation V.18(a,b) are modified to take into account a second optical mode interacting with the electrons:

$$\delta P_1(t) = -\Gamma_{P_1} \cdot \delta P_1(t) + \sigma_{N \to P_1} \cdot \delta N(t)$$

$$\delta P_2(t) = -\Gamma_{P_2} \cdot \delta P_2(t) + \sigma_{N \to P_2} \cdot \delta N(t) + \eta_c \cdot \frac{P_{in}(t)}{h\nu}$$

$$\delta N(t) = -\Gamma_N \cdot \delta N(t) - \sigma_{P_1 \to N} \cdot \delta P_1(t) - \sigma_{P_2 \to N} \cdot \delta P_2(t)$$

Equation V.30

with the input beam matching the second cavity mode. The modified circuit is given in Figure V.4 [28] with the appropriate component values.

In the modified circuit, the cavity mode that is under external optical modulation has a frequency pole at (R_{p2} / L = Γ_{p2}) and is now interacting with two frequency poles in parallel: the pole due to the electrons at (1 / R_nC = Γ_n) and the one due to the other optical mode at (R_{p1} / L = Γ_{p1}). Repeating the previous derivation, an

expression for the amplifier gain as a function of modulation frequency (similar to Equation V.22) is obtained:

$$\text{Gain} = \frac{\eta_c \alpha_m \left[\left(\Gamma_n + i\omega_m\right) + \dfrac{1}{\sigma_{n\to p_2}\sigma_{p_1\to n}\left(\Gamma_{p_1} + i\omega_m\right)} \right]}{\left[\left(\Gamma_n + i\omega_m\right) + \dfrac{1}{\sigma_{n\to p_2}\sigma_{p_1\to n}\left(\Gamma_{p_1} + i\omega_m\right)} \right] \left(\Gamma_{p_2} + i\omega_m\right) + \left(\sigma_{n\to p_2}\sigma_{p_1\to n}\right)}$$

Equation V.31

Note that if mode 1 is not close to its threshold, Γ_{p1} increases, and the first term in the square brackets dominates the second term, reducing Equation V.31 to Equation V.22 (i.e. single mode operation).

Conversely, if mode 1 is at its threshold, the second term in the square brackets in Equation V.31 will dominate the first term in the square brackets. This means that the optical mode under modulation will be amplified at the expense of the other optical mode rather than the electrons. In other words, the carrier density stays the same and the output light intensity of mode 1 drops as the intensity of mode 2 increases. Following the steps from Equation V.22 to Equation V.29, we arrive at the modified gain-bandwidth product of the amplifier with two cavity modes at their thresholds at the given bias point:

$$\text{GBW}_{\text{max imum}} \cong \frac{\sqrt{3}\eta_c \cdot \alpha_m}{4\pi}$$

Equation V.32

Comparing Equation V.32 with Equation V.29, the gain-bandwidth product is reduced by a factor of ($\sqrt{3}$/4). A factor of ($\sqrt{3}$/2) comes from the fact that when calculating Equation V.29, the expression in curly brackets in Equation V.28 was computed to be between 1.73 (=$\sqrt{3}$) and 2.23 and it was approximated to an average value of 2. In the case of an amplifier where the gain for one optical mode comes from the other optical mode rather than the electrons, that value is always ($\sqrt{3}$), so Equation V.29 is modified by ($\sqrt{3}$/2). In Equation V.32, there is an additional factor of 2 in the denominator, which is due to the fact that the current flow in Figure V.4 is now through the inductor of mode 1 rather than the R_nC branch. Then, as the modulation frequency is increased, the impedance of the overall current loop increases with $2\omega_m$ compared to only ω_m of the single mode amplifier. This is because each inductor contributes an imaginary part of ω_m to the impedance, and in the case of multimode operation, the current flows through two inductors in series.

V.3.1.2. Gain - bandwidth tradeoff in positive feedback amplifiers

Before we start discussing the experimental verification of the above theory, we note the similarity between the gain-bandwidth expression of a VCSEL amplifier,

and that of its electronic counterpart, the avalanche photodiode (APD). The GBW product of an APD is [29]:

$$GBW_{APD} = \frac{1}{2\pi \cdot N \cdot k \cdot \tau_0}$$

Equation V.33

where N is a correction factor, k is the ratio of ionization rates for electrons and holes ($k < 1$), and τ_0 is the transit time of carriers through the avalanche region. As is the case for all amplifiers with positive feedback, the GBW product is proportional to the inverse of the carrier lifetime (i.e. the transit time). Similarly in a VCSEL amplifier, the photons in the cavity experience amplification. Since only the photons that are lost through the output mirror contribute to the output light power, the lifetime of the output photons is simply the inverse of α_m. Thus apart from a constant factor, Equation V.29 and Equation V.32 are equivalent with Equation V.33.

This common behavior in VCSEL amplifiers and avalanche photodetectors can be qualitatively explained by the general tradeoff between the gain and the bandwidth in all positive feedback amplifiers (whether they are optical or electrical). By positive feedback, we mean a device where when one carrier (i.e. a photon in an optical amplifier and an electron or hole in an electrical amplifier) gets generated from another carrier, it stays in the same medium, and keeps on generating new carriers as in a geometric series.

As an example, consider an optical amplifier where the average lifetime of an output photon is τ_{out}. Here, we make the distinction between the lifetime of a photon and that of an 'output' photon such that an output photon is one that gets collected by the detector. Then, the lifetime of a photon would be a combination of all the loss mechanisms including the mirror loss through the output mirror:

$$\frac{1}{\tau_{total}} = \frac{1}{\tau_{out}} + \frac{1}{\tau_{mirror2loss}} + \frac{1}{\tau_{scatteringloss}} + \ldots$$

Equation V.34

Now, consider inputting one photon every τ_{out} second. Each photon generates 'r' photons ($r < 1$) within τ_{out} seconds before they exit the cavity, and then the newly generated 'r' photons generate 'r^2' within the next τ_{out} seconds, and so on (Figure V.6). At the same time, there is another 1 photon being input every τ_{out} seconds, so at steady-state equilibrium, there will be [1 / (1-r)] photons being output at any one time. This number constitutes the steady-state gain of the cavity, and is obtained by simply adding all the terms of a geometric series with the first number equal to one and the ratio of consecutive numbers is 'r'.

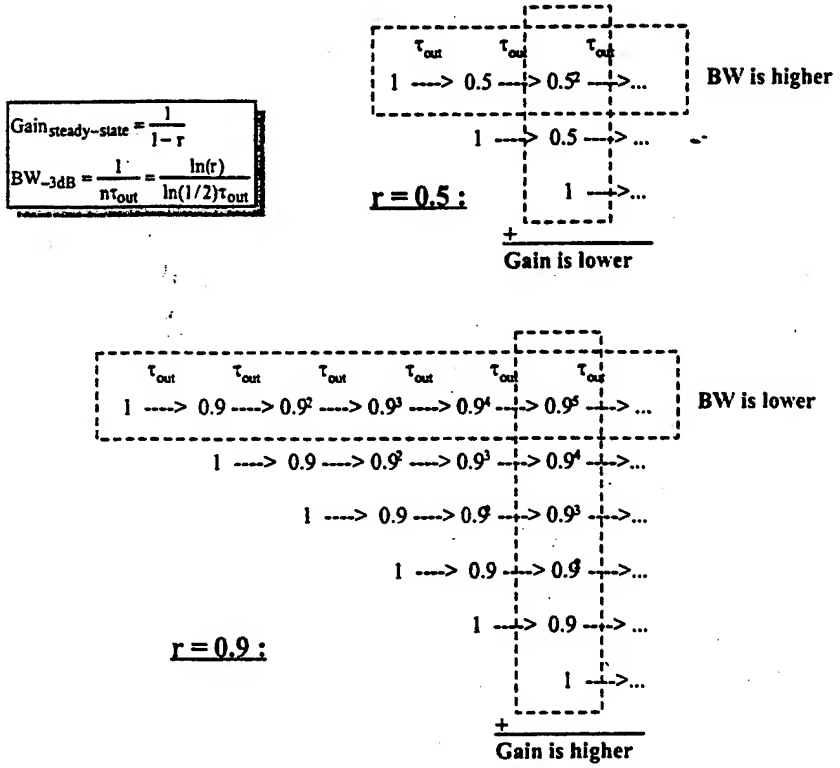


Figure V.6 Gain - bandwidth tradeoff in positive feedback amplifiers.

One can immediately see that to have a high steady-state gain, 'r' needs to be closer to unity. However, in that case, the geometric series requires more terms to reach 50% of its total value. This, in turn, means that it will take more time steps (each step being equal to τ_{out} seconds) until that 50% is built up in the cavity. As a result, the bandwidth decreases: -3dB bandwidth is equal to the inverse of the product of the number of steps required and the duration of each step.

In summary, to have more gain, one requires more steps, which decreases the bandwidth, and vice versa. The overall gain-bandwidth product will be proportional to the duration of each time step, or more precisely, to its inverse. This is why the gain-bandwidth product of the VCSEL amplifier and that of the APD are both proportional to the inverse of the lifetime of the carriers (i.e. photon in the VCSEL and electron/hole in the APD).

V.3.2. Experiment

The VCSEL used in the experiments was designed to operate as a transmitter, so it is not an optimum amplifier (i.e. an amplifier would be designed to maximize its gain-bandwidth product rather than its output power). However, the device structure is practically the same for both a transmitter and an amplifier, so by properly biasing the device, we can use it to verify our theory presented in Section V.3.1.

The device used in our experiments is a top-emitting, proton-implant VCSEL with three GaAs/AlGaAs quantum wells embedded in a 1-λ long cavity, lasing at around λ = 852 nm. The cavity diameter is 15 μm, and the properties for the two mirrors are: (R_1=99.47%, T_1=.37%, A_1=.16%), and (R_2=99.85%, T_2=0%, A_2=.15%) [30]. The device is on an absorbing substrate, so mirror 1 acts as both the input and the output mirror (i.e. the device is operated in the reflection mode).

A tunable Ti:Sapphire laser (optically pumped by an Argon ion laser) is used as the source, where the beam is in the fundamental Gaussian mode. The VCSEL's experimental LI curve and IV curve are given in Figure V.7. The VCSEL exhibits two spatial modes with orthogonal polarization from its threshold (~3 mA) until about 5.5 mA. At this point (i.e. where the kink is on the LI curve in Figure V.7), it experiences mode hopping and its two spatial modes change to two other spatial modes, again with orthogonal polarization (Figure V.8). Since the light from the Ti:Sa laser is in the fundamental mode, it is run through a polarizer before input into the amplifier such that the input mode will exactly match the bottom right mode in Figure V.8, and the optimum biasing point is expected to be around ~5.5mA.

At the bias current of ~5.5mA, two modes reach their thresholds and begin to lase simultaneously with approximately equal output intensities, so Equation V.32 needs to be used for the gain-bandwidth product of the amplifier (i.e. a two-mode amplifier). Substituting the mirror reflectivities in Equation V.13 and assuming the input beam's frequency is resonant with the cavity, the input coupling efficiency is calculated to be 48%. Assuming the average penetration depth of the field into the mirrors is 1 λ [31], the effective cavity length in Equation V.20 becomes 3 λ, so substituting Equation V.13 and Equation V.20 in Equation V.32, we calculate the theoretical upper limit for the gain-bandwidth product of this amplifier to be 14.4 GHz.

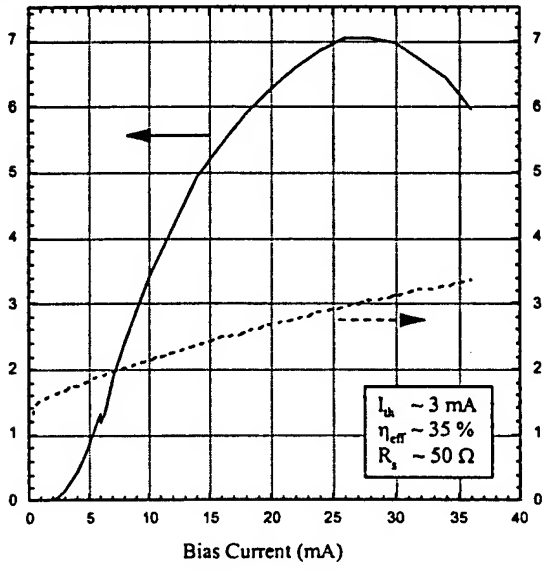


Figure V.7 LI and IV curves of the VCSEL used for the experiments.

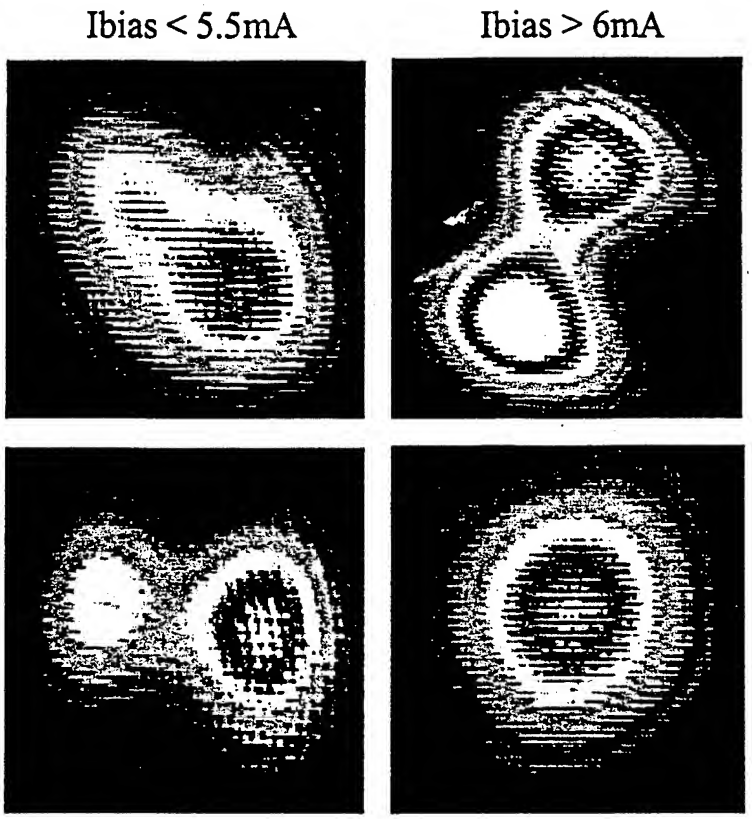


Figure V.8 Spatial and polarization modes of the VCSEL used for the experiments.

V.3.2.1. Optical setup for the experiments

The optical setup used for the experiments is given in Figure V.9. The diameter of the VCSEL amplifier was only 15μm and the cavity was a very high Q Fabry-Perot cavity. Therefore, the input beam needs to be on-axis, and both the xyz translation and the 2-axis tilt of the device need to be controlled very precisely to be able to couple the input beam into the VCSEL amplifier. To achieve high coupling efficiency, each component is brought into the optical setup one by one in a methodical fashion, where the alignment of each component is verified before the next component is brought in.

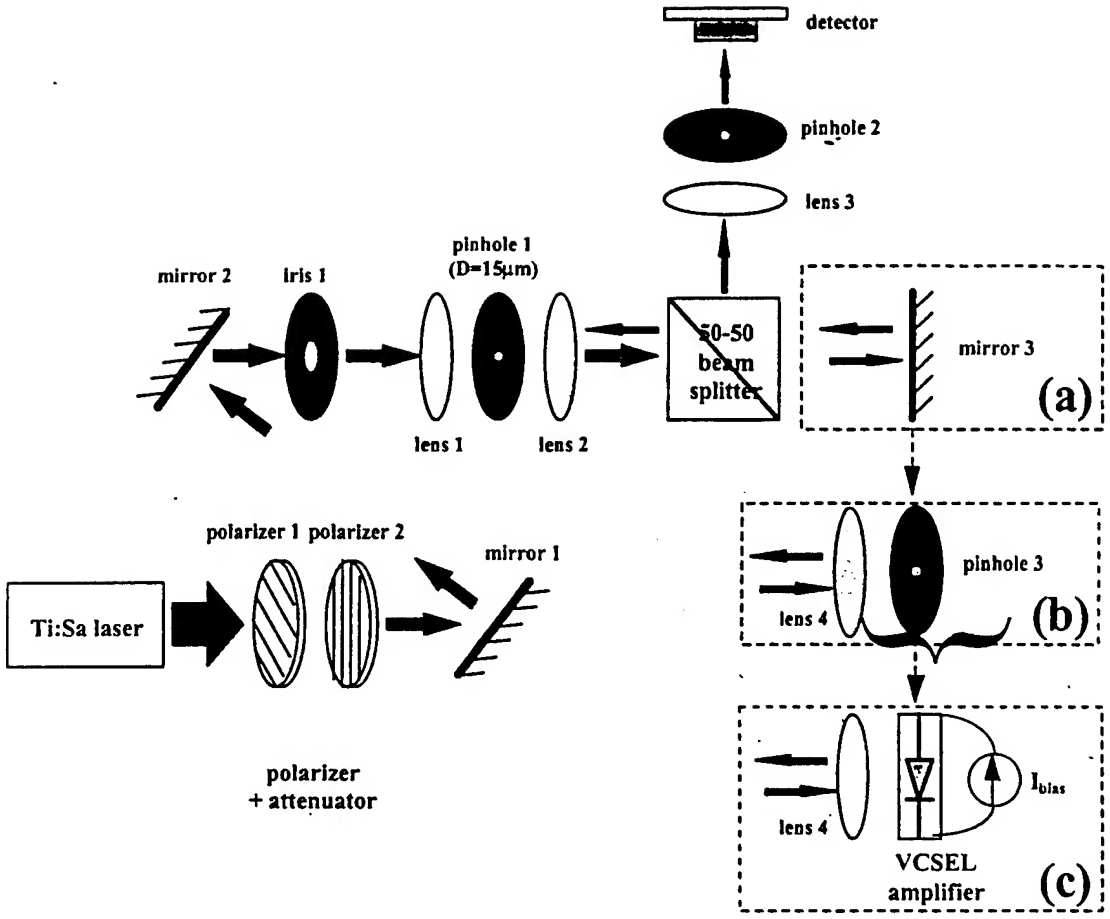


Figure V.9 Optical setup used for the experiments.

In Figure V.9, the Ti:Sa laser is used as the input beam. Polarizer 2 is used to control the direction of the input beam's polarization going into the VCSEL amplifier, and the addition of Polarizer 1 allows us to control the input intensity (e.g. when the two polarizers are orthogonal, input intensity drops to zero). Mirror 1 and Mirror 2 allows us control on the direction of the optical axis. Iris 1 is used for alignment purposes as will be explained below.

After Iris 1 is placed, Mirror 3 is positioned (Figure V.9(a)) such that the reflection from that mirror hits Iris 1 in the center (i.e. Mirror 3 is perpendicular to the optical axis). Next, the beam-splitter is brought in, and the Mirror 3 is adjusted to account for the slight tilt that the two faces of the beamsplitter might have with respect to each other. Since the diameter of Iris 1 is on the order of millimeters, this is just a crude alignment, and is in no way sufficient to align the VCSEL amplifier (which requires micron accuracy).

Next step is to bring the pinholes into the setup, where the diameters of the pinholes are comparable with that of the VCSEL, such that finer adjustments can be made. First, pinhole 2 is placed on the optical axis by maximizing the light throughput

without a lens in front (i.e. without 3). Then, lens 3 is positioned to again maximize the light throughput out of pinhole 2. This ensures that both pinhole 2 and lens 3 are on-axis. Second step is the placement of the spatial filter before the beamsplitter. Again, pinhole 1 is placed initially, and the light throughput is maximized to make sure that it is on-axis. Then, lens 1 and lens 2 are placed, each time maximizing the light throughput out of pinhole 2. The spatial filter serves two purposes. The first one is to clean up the spatial profile of the input beam to increase the coupling efficiency. The second (and more important) one is to ensure that the beam incident on mirror 3 and the one reflected from it are collinear within micron accuracy. The reason is that if there is a slight tilt between the two beams, then the reflected beam does not go through pinhole 1 and cannot be seen at Iris 1. This gives us a way to verify that mirror 3 is perpendicular to both the incident and the reflected beams with an accuracy that is sufficient for coupling into the amplifier.

The final step is the placement of the amplifier. For this, mirror 3 is taken out of the setup, and pinhole 3 is centered on the optical axis by maximizing its power throughput without a lens in front (Figure V.9(b)). Then, lens 4 is placed, again maximizing the power so that lens 4 is centered on-axis and perpendicular to it. Finally, pinhole 3 is taken out, and the VCSEL amplifier is put in its place (Figure V.9(c)), which sits on a 5-axis positioner. Since the amplifier needs to have the right xyz position and the right 2-axis tilt, this is done in two steps. First, the amplifier is turned off, and its surface is used as a planar mirror. By reflecting the Ti:Sa light from the amplifier's input surface, and making sure that the reflected light is centered on iris 1 (i.e. that it passes through pinhole 1), the tilt of the amplifier is aligned accurately. Then, the Ti:Sa is turned off and the VCSEL is turned on (i.e. operated not as an amplifier but as a transmitter). Again, by ensuring that the VCSEL output is centered on iris 1, the xyz position of the amplifier is aligned with micron accuracy (since otherwise, the VCSEL output would be blocked by pinhole 1). Now, the VCSEL is biased below threshold, the Ti:Sa is turned back on, and the system is ready for the experiments.

V.3.2.2. Steady-state gain

Figure V.10 shows the steady-state cavity gain versus bias current in response to 2.7 μW input power. The reported cavity gain does not include the input coupling efficiency. As an example, if 2.7 μW of light is input, and η_c is calculated to be 48%, then only 1.3 μW gets coupled into the cavity. If the cavity gain is 100 then the output power is 130 μW, so the ratio of output to input power is in fact the cavity gain multiplied by the coupling efficiency.

As predicted in section V.3.1, the gain of the amplifier increases as the bias current is increased to the optical mode's threshold, where it reaches a maximum. As the bias current exceeds the mode threshold, Ω_R^2 in Equation V.25(b), which is proportional to the number of photons in that mode, quickly increases and the cavity gain drops down to unity. The decrease in the other optical mode's output power is also plotted. It can be seen that the decrease in that mode is almost the mirror image of the gain for the input beam, which justifies the use of Equation V.32 instead of

Equation V.29 because the gain comes from the other optical mode rather than the electrons.

To find the small-signal gain to be used in calculating the gain-bandwidth product, we measured the steady-state cavity gain as a function of the input light intensity with the bias current equal to the mode's threshold (i.e. at 5.5 mA) (Figure V.11). Fitting a curve to the measured data points according to the general equation for gain saturation in a laser:

$$\text{gain} = \frac{\text{gain}_{max}}{1 + \frac{L_{in}}{L_{sat}}}$$

Equation V.35

where gain_{max} is the asymptotic maximum value of the small-signal gain and L_{sat} is the saturation input intensity (i.e. when the gain drops to one half of its maximum value), we obtain $\text{gain}_{max} = 238$ and $L_{sat} = .85\ \mu W$. The decrease in the other optical mode's output power is plotted again to justify the use of Equation V.32 in the presence of two optical modes.

V.3.2.3. Bandwidth

Since the VCSEL used in our experiments was designed to operate as a transmitter, the reflectivity of both mirrors are unequal and are very high, which makes the amplifier operation very sensitive to the wavelength of the input beam. If a modulated laser beam is used as the source for the bandwidth measurements, the frequency chirping of the source output would modulate the input coupling efficiency of the amplifier and would make it impossible to verify the theory of section V.3.1 in a reliable way. As another alternative, if the input beam were modulated with a modulator, the low contrast ratio of these modulators would suffer from the saturation of the gain (from Equation V.35), and again render the results useless.

As a result, we used an indirect method to measure the -3dB bandwidth, where the input beam is kept constant at the resonant wavelength, and instead the bias current of the amplifier is modulated. This modulates the carrier density inside the cavity, which modulates the resonant frequency. Since the input beam's frequency is kept constant, the input actually couples into the cavity and gets amplified only when it matches the resonant frequency of the cavity. To illustrate the point, the detected output intensity of a VCSEL amplifier is shown in Figure V.12, where this amplifier is single-mode with the mode threshold equal to the device threshold. Figure V.12(a) is when the input is zero such that the background output of the amplifier is measured. Figure V.12(b)-(d) shows the amplified signal superimposed on the background output as the wavelength of the input beam is increased. Since increasing the bias current of the amplifier increases the carrier density inside the cavity and increases the effective optical length of the cavity, the resonant frequency is lowered, so an input with a higher wavelength can couple into the cavity and experience amplification at a higher bias current. Furthermore, the amplitude of the amplified signal increases because the

gain increases as the bias current gets close to the optical mode's threshold, which is also the device threshold in this case.

As the modulation frequency of the bias current is increased, the curve for the background output intensity stays the same, but the amplifier bandwidth begins to limit the amplitude of the superimposed amplified signal. In other words, once the input beam becomes resonant with the cavity, it couples into the cavity. However, before it can be fully amplified, the resonant frequency of the cavity changes again, and the input coupling efficiency drops back to zero. Measuring the decrease in the amplitude of the amplified signal (relative to its steady state value) and the actual time that the resonant cavity frequency sweeps the input beam's frequency, one can calculate the -3dB frequency of the amplifier.

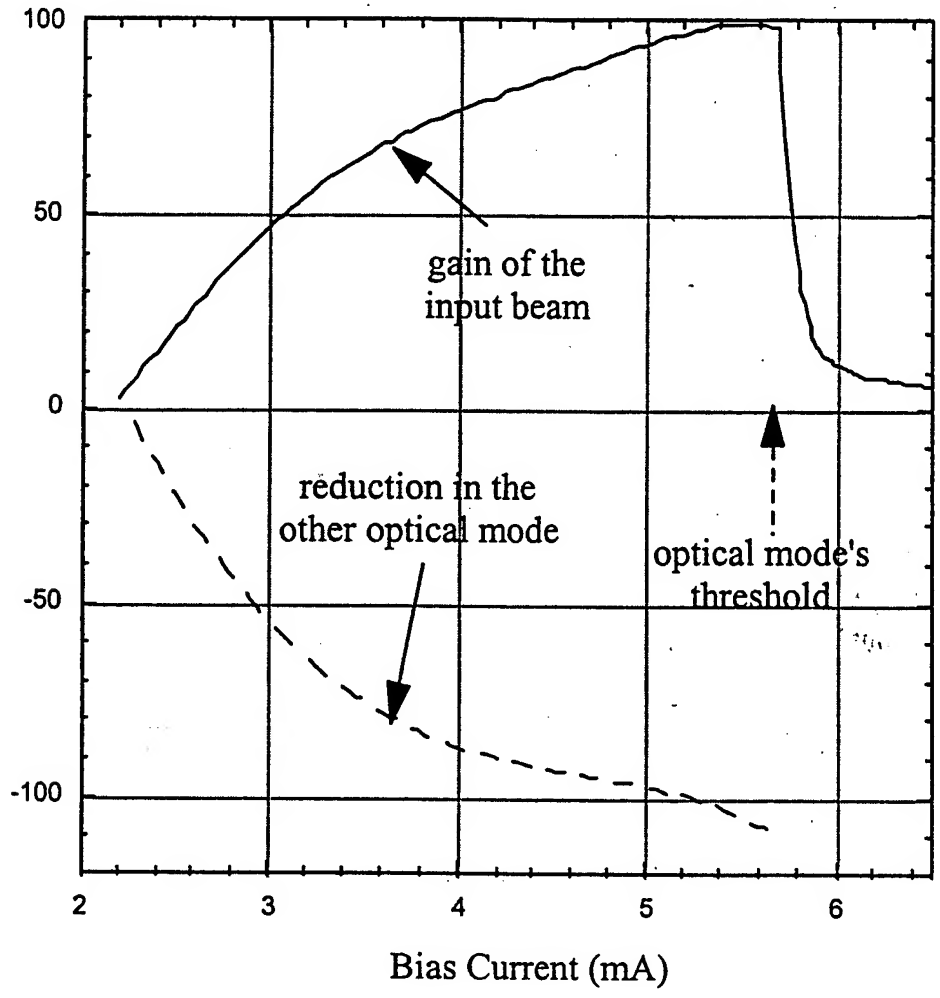


Figure V.10 Steady state cavity gain vs. bias current for 2.7 μW input light intensity.

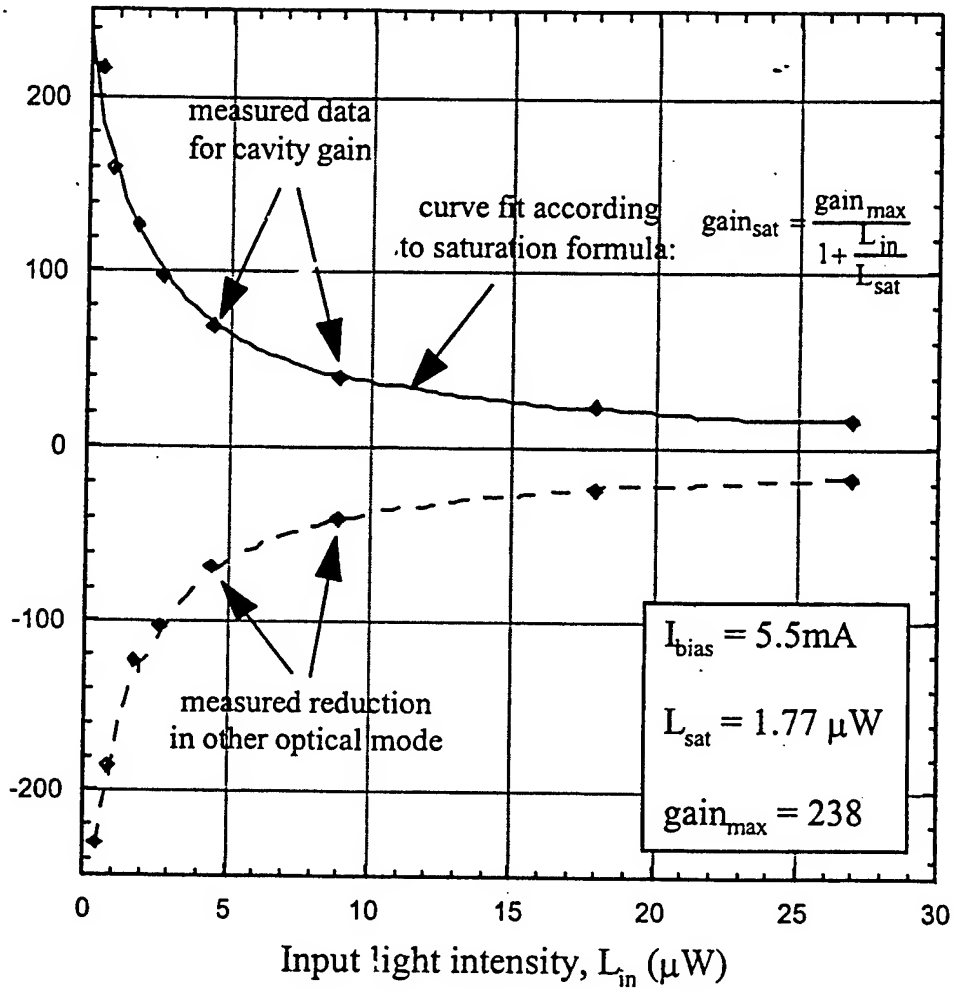


Figure V.11 Steady state cavity gain versus input light intensity (i.e. light coupled into the cavity / input coupling efficiency), and curve fitting according to the saturation formula to obtain maximum gain and saturation intensity of the amplifier.

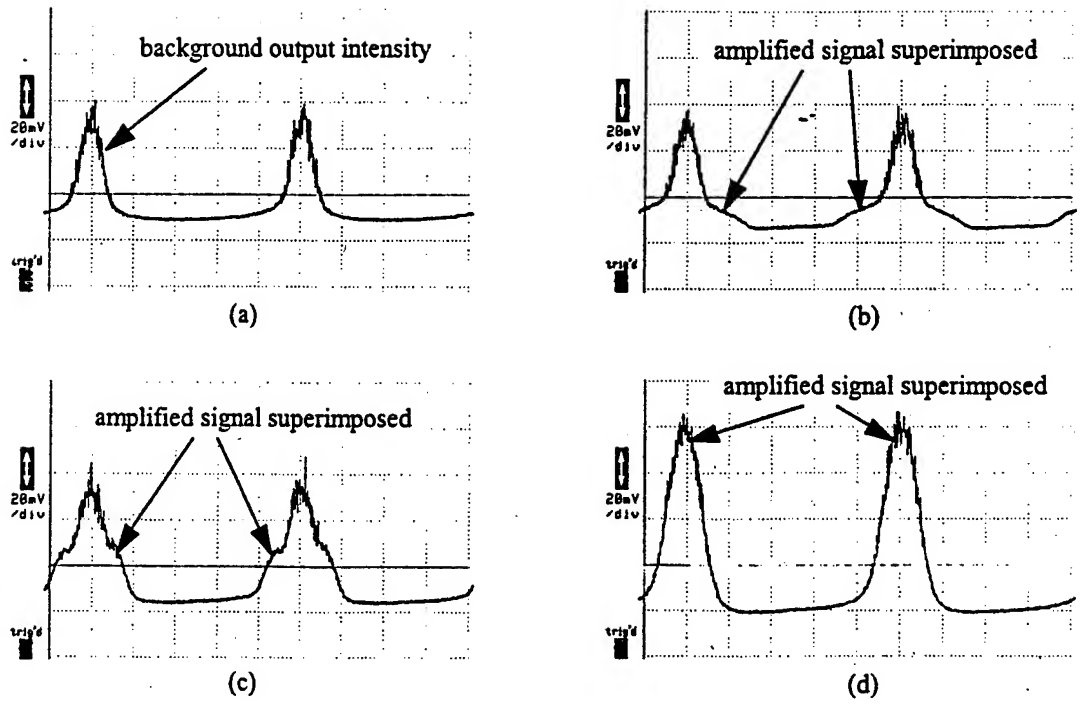


Figure V.12 The output intensity of a VCSEL amplifier with its bias current modulated around its threshold: (a) with no input to show the background output of the device, (b)-(d) with the amplified signal superimposed. As the input beam's wavelength is increased in (b) through (d), it couples into the cavity at a higher carrier density (i.e. at a higher bias current). The amplitude of the amplified signal also increases since the gain increases as the bias current gets closer to the device threshold, which in this case is also the optical mode's threshold.

Using a simple pole approximation, the -3dB frequency of the amplifier is:

$$f_{-3dB} = \frac{1}{2\pi} \cdot \frac{\ln\left(\frac{1}{1-f}\right)}{t_0}$$

Equation V.36

where f is the reduced amplitude of the amplified signal normalized to its steady-state value, and t_0 is the time it takes to go from zero to its maximum value. For the specific VCSEL used in the steady state gain experiments, when it is biased at the optical mode's threshold (i.e. at ~ 5.5mA), the amplitude of the amplified signal drops to .5 of its steady state value in 1 ns. Using Equation V.36, the -3dB frequency is calculated to be 110 MHz.

V.3.3. Discussion

From Equation V.32, our theory predicts the upper limit of the VCSEL amplifier's gain-bandwidth product to be 14.4 GHz. From the experiments, the maximum steady-state cavity gain of the amplifier is measured to be 238, the input coupling efficiency is calculated to be 48%, and the -3dB bandwidth at threshold is measured at 110 MHz, which gives a maximum gain-bandwidth product of 12.6 GHz. The maximum gain-bandwidth product experimentally measured is approximately 90% of the value predicted from our theory. Including the fact that any misalignment in the optical system will reduce the measured values, this result indicates the validity of our theory.

From Equation V.29 and Equation V.32, to increase the gain-bandwidth product of a semiconductor amplifier, one needs to increase the photon loss rate through the output mirror (α_m). From Equation V.20, the cavity length of the VCSEL is dictated by the wavelength of the desired light output, so to increase the GBW product, one needs to reduce the reflectivity of the output mirror. In this case, the other mirror reflectivity needs to be reduced to approximately the same value so that the input coupling efficiency (η_c), which decreases with unequal reflectivities, does not drop. Furthermore, there is a lower limit on the mirror reflectivities due to the fact that the maximum GBW product is achieved when the amplifier is biased at threshold. If the total optical gain of the device cannot compensate for the total mirror loss, the bias point moves away from the laser threshold and the performance of the amplifier drops very quickly.

Assuming the input beam is in a polarized fundamental spatial mode, the maximum gain-bandwidth product would be obtained with a VCSEL amplifier that has only the polarized fundamental spatial mode at the device's threshold. We assume a 1 λ-cavity with three 85 Å-thick quantum wells placed at a resonant peak of the standing wave inside the cavity and the device is biased at its threshold. If the optical gain of the quantum wells is 1000 cm^{-1}, the optimum mirror reflectivity would be 99.3% for the output mirror and 99.7% for the other mirror to give a gain-bandwidth product of 111 GHz. In these calculations, we assume that the absorption in the mirrors is negligible and that the total mirror loss dominates the rest of the cavity

losses. If the optical gain in the quantum wells can be increased to 5000 cm^{-1}, the optimum structure would be an output mirror at 96.7% and the second mirror at 98.3% for a 556 GHz gain-bandwidth product.

As presented above, the performance (i.e. GBW product) of the VCSEL amplifiers is very promising. In terms of practical implementation, midsize VCSELs (10 - 25 μm diameter) are preferable over smaller VCSELs to increase the alignment tolerance of the required optical system. However, as mentioned in section V.3.1, midsize VCSELs typically have multiple modes that would degrade the amplifier performance. Furthermore, the nonuniformity of spatial modes across a large array of VCSELs would preclude the use of VCSEL amplifiers for large-scale applications. To solve this problem, a post-fabrication annealing procedure has been proposed and experimentally demonstrated on proton-implant VCSELs [32] to eliminate any asymmetries in their gain mediums such that they all exhibit only the fundamental spatial mode at their thresholds.

In addition to the spatial mode control of VCSELs, their polarization needs to be selectively controlled. Previously several solutions have been proposed that include either changing the physical shape of the cavity or one of its layers (e.g. the oxide aperture) to a rectangle, an ellipse, or any other asymmetric shape [33,34], or introducing an asymmetry into the gain and/or the loss mechanisms [35,36].

Another issue for the VCSEL amplifiers is the sensitivity of the input coupling efficiency to the frequency chirping of the source, but reducing the mirror reflectivities to increase the gain-bandwidth product of the amplifier also increases the linewidth of the device. For the proposed amplifier structure above with ~98% mirror reflectivities, the -3dB linewidth of the amplifier is calculated to be around 2 nm. Since the frequency chirping of a VCSEL source is on the order of a few angstroms, this mismatch will get naturally resolved with an optimal VCSEL amplifier structure.

Finally, the common issue with all optical amplifiers is the modal noise, but due to their short cavity lengths, VCSELs operate in a single longitudinal mode. With the approaches mentioned above to control the spatial mode and the polarization of a VCSEL, it is feasible to have a single mode device, and thus eliminate the mode-partitioning noise.

V.3.4. VCSEL as an optical modulator

Based on the method used to do the bandwidth experiment (section V.3.2.3), the structure proposed for the VCSEL amplifier in section V.3.3 can also be used as an ultra-low voltage, high speed, high contrast ratio optical light modulator with an expected performance of > 1 GHz bandwidth, > 10:1 contrast ratio, and < 50mV modulation voltage [37].

As silicon CMOS technology parameters are scaled down and standards for logic voltage levels are reduced, present optical transmitter technologies including the multiple-quantum-well (MQW) modulators and the vertical cavity surface emitting lasers (VCSELs) will become incompatible with silicon interconnects because of their high drive voltage requirements. Thus a device structure capable of modulating light effectively with ultra small voltage swings and bias currents that can be integrated

with future silicon technologies will play an important role in the future of optical interconnects.

Many optical system applications of the future may require the use of both modulators and microlasers within the same system. MQW-modulators have an advantage over active light emitters in terms of signal and clock distribution [38] since they allow pulsed operation. In these systems, the clock can be distributed optically to eliminate the clock skew and jitter problem, which exists in all large-scale systems. Also, the electrical signals can be sampled with short optical pulses to improve the performance of receivers [39]. However, the MQW modulators suffer in terms of contrast ratio of the optical output power as the CMOS technology is scaled down and the supply voltage is reduced. VCSELs, on the other hand, are forward biased diodes and the applied current depends exponentially on the voltage across the device, so better contrast ratio can be achieved for the same voltage levels. However, the device needs to be biased above threshold to reduce the turn-on time delay, and to maintain a high contrast ratio, the modulation current swing needs to be increased, which reduces the system bandwidth and increases the power dissipation.

Another application for low-voltage light modulators is superconductor devices where current is easily achievable, but because of the near zero impedance of the environment, voltage swings are limited to a few tens of millivolts. In this case, using a VCSEL amplifier as a high-contrast ratio light modulator with a ~50mV modulation voltage may be the ideal solution to bring optics into a superconducting environment.

To do the bandwidth experiments, we had kept the input light beam constant and modulated the bias current of the VCSEL amplifier (Figure V.12). The same setup can be used but now, with the VCSEL operated as a light modulator instead of an amplifier. The principle of operation, the VCSEL structure, and the biasing conditions are exactly identical. The only condition is that the VCSEL needs to be modulated between two levels where the low level will be approximately 1 mA below its threshold to ensure that the input light does not couple into the cavity due to the resonant frequency mismatch. The high level, on the other hand, will be slightly below its threshold current (as close to it as possible without lasing). The input frequency will match the resonant frequency of the cavity at this bias current.

Under these conditions, when the modulation current is low, the incident beam will be reflected from the front mirror, constituting the low level for the modulator output. On the other hand, when the modulation current is at its peak, the incident beam will become resonant with the cavity, couple in, and experience amplification, so that the high level for the modulator output will be the amplified signal. The contrast ratio will then be the amplification factor (assuming spontaneous emission power is negligible). Furthermore, because of the active cavity (i.e. amplification), the modulator effectively operates with zero insertion loss.

Due to the high reflectivities of the VCSEL structure, approximately 1 mA of modulation current is sufficient to make the input light frequency off resonant with the cavity. Considering the series resistance of the VCSEL to be ~ 50 Ω, only 50 mV of voltage swing is enough for the modulator to operate with a high contrast ratio.

Furthermore, since the mirror reflectivities are reduced to increase the gain-bandwidth product of the amplifier, the linewidth of the input coupling efficiency is also increased. For the above mentioned mirror reflectivities, the FWHM linewidth of the input light's wavelength is > 2nm, which is sufficient to allow the coupling of a few hundred femtoseconds or longer pulses (i.e. it allows pulsed operation for improved synchronization, optical clock distribution, etc.).

V.4. Amplifier bandwidth

In the previous two sections, we have shown that the polarization and the spatial mode of VCSELs can be selectively controlled. The last step to show that device uniformity is not a problem to prevent the insertion of VCSEL amplifiers into large systems, we show that the longitudinal modes across an array are also uniform enough for VCSEL amplifiers.

Amplifier bandwidth is defined as the full width of the input light's frequency where the gain of the amplifier drops to 50% of its peak value (i.e. FWHM). To find the full width, we start from the coupling efficiency of the device given in Equation V.13 (repeated below for convenience)

$$\eta_c = \frac{T_1(1-R_2)}{1+R_1R_2-2\sqrt{R_1R_2}\cos\delta}$$

Equation V.37

δ is the mismatch between the input frequency and the resonant cavity frequency. For the VCSEL used in the experiments of section V.3.2, the mirrors had (R_1=99.47%, T_1=.37%, A_1=.16%), and (R_2=99.85%, T_2=0%, A_2=.15%). Plugging these values into Equation V.37 predicts the full width at half maximum of the coupling efficiency to be ~9.2 Å.

The measured full width at half maximum of the amplifier bandwidth is ~3.0 Å. The discrepancy between the predicted and the measured amplifier bandwidths comes from the fact that Equation V.37 is the coupling efficiency into a 'passive' Fabry-Perot cavity. Therefore, it does not take into account the additional phase shift introduced by the cavity gain. From the Kramers-Kronig relations, every absorption and/or stimulated emission of a photon by an atom introduces an additional phase shift to the optical field. The reader is referred to any textbook on the quantum interaction between photons and atoms for a discussion of Kramers-Kronig relations (e.g. [40]). As a result of this additional phase shift, semiconductor laser amplifiers experience gain narrowing, where the amplifier bandwidth is decreased from the atomic gain spectrum by a factor dependent on the amplifier gain. A plot of reduction in the amplifier bandwidth as a function of amplifier gain is shown in Figure V.13 [41]. From the figure, the bandwidth of an amplifier with ~20 dB gain is approximately 35% of the value if the phase shift due to amplification was neglected. Combining this with the predicted 9.2 Å FWHM of the coupling efficiency, the amplifier bandwidth becomes ~3.2 Å, which is in line with the measured value (i.e. ~3.0 Å).

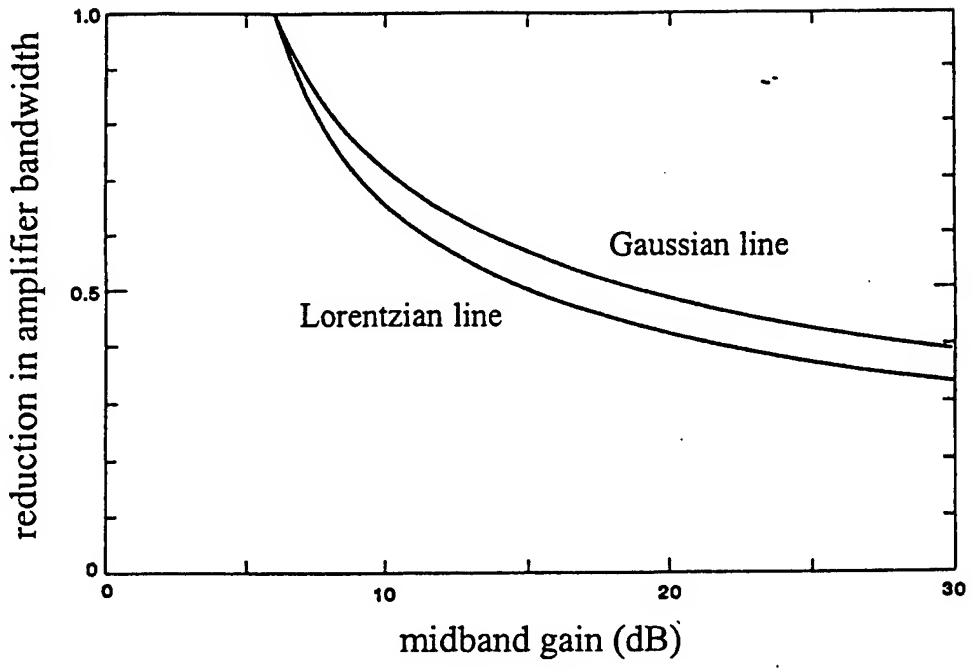


Figure V.13 Reduction in amplifier bandwidth vs. amplifier gain due to gain narrowing.

The next step is to calculate the amplifier bandwidth for an optimum VCSEL amplifier structure as proposed in section V.3.3. For a cavity with an optical gain of 5000 cm^{-1} in the quantum wells, the reflectivities of the output and the second mirror was predicted to be 96.7% and 98.3% to maximize the gain-bandwidth product of the amplifier. Using these numbers in Equation V.37 and the additional gain narrowing factor of ~ 35% from Figure V.13 (assuming ~20 - 25 dB gain), the predicted amplifier bandwidth is ~24 Å. At the present, arrays of VCSELs can be fabricated where the wavelength variation is less than ~8 Å [42,43]. As a result the optimum VCSEL amplifier structure, proposed earlier for maximum gain-bandwidth product, will provide a sufficient amplifier bandwidth such that controlling the longitudinal frequency across a large array of VCSEL transmitters will not constitute a problem.

V.5. Noise performance

In this section the noise performance of VCSEL amplifiers is addressed. In all laser amplifiers, there is an inherent limitation on the minimum input power that can be reliably amplified and detected because of the spontaneous emission in the lasers. Since spontaneous emission is random by nature, it leads to the main sources of noise in all optical laser amplifiers.

The first source of noise is the mode-partitioning noise in multi-mode lasers, where the power in one mode fluctuates and causes the power in another mode to fluctuate as well, leading to a smaller SNR ratio for that particular mode. For a

discussion of mode-partition noise, refer to [44] or the references listed therein. In this case, VCSEL amplifiers have a clear advantage over other optical amplifiers because due to their very short cavity lengths, only a single longitudinal mode can exist. Operating the VCSEL as a single-mode laser eliminates the mode-partitioning noise in VCSEL amplifiers.

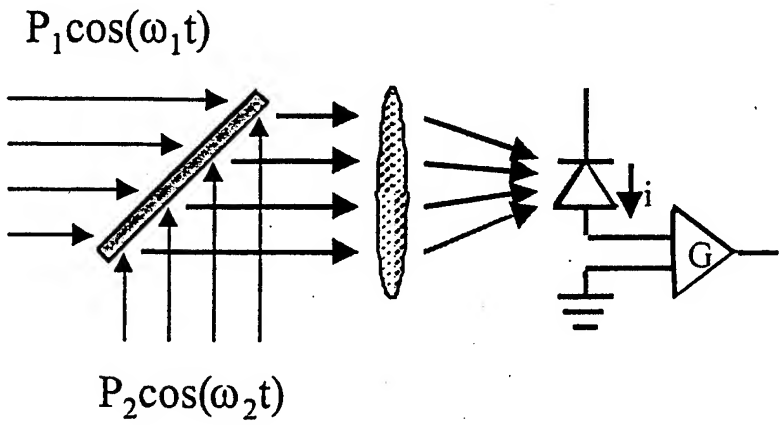


Figure V.14 A typical optical heterodyne detection.

The second and the most dominant source of noise of an optical amplifier (that operates in a single-mode) is the receiver noise due to the beating of the signal and the spontaneously emitted photons at the detector [45], similar to optical heterodyne detection (Figure V.14). In optical heterodyne detection, an input signal of low power (P_1) with an optical frequency of ω_1 is interfered with a second optical signal of high power (P_2) and a slightly different optical frequency of ω_2. The resulting electrical current at the detector is

$$i_{detector} = \frac{q\eta_{qe}}{h\nu}\left[\begin{array}{l} P_1 + P_2 + 2\sqrt{P_1 P_2}\cos(\omega_1 - \omega_2)t \\ +P_1\cos 2\omega_1 t + P_2\cos 2\omega_2 t + 2\sqrt{P_1 P_2}\cos(\omega_1 + \omega_2)t \end{array}\right]$$

Equation V.38

The first two terms are dc values, so they can be filtered out with a suitable filter. The terms in the second row are all at optical frequencies, so the electronics cannot react to those terms, and thus they are averaged out to zero. The remaining term (i.e. last term in the first row with ω_1 - ω_2 dependence) is the one of interest, where the amplitude of the current is proportional to P_2. Since P_2 can be increased arbitrarily (as long as the signal to noise ratio is acceptable), amplification is achieved for the detection of P_1.

In the case of the VCSEL amplifier, the mathematics behind the beating noise is exactly the same as the one for optical heterodyne detection except that the second beam is not an external source but is due to the spontaneously emitted photons.

V.5.1. Conversion of SNR to BER

The required noise performance of a system is expressed in terms of a bit-error-rate (BER), which indicates the frequency that can be tolerated for having a bit detected incorrectly after transmission. For typical voice communication systems the BER is around 10^{-9} - 10^{-10}, and for data communication systems the required BER is decreased to 10^{-12} - 10^{-15}. Depending on the transmission bandwidth, the BER determines how often an error will occur.

The BER of a given system can be derived from the signal-to-noise ratio (SNR) of each component in the link, and this ratio is usually dependent on the input and output signal levels for each component. In a free-space optoelectronic link without an optical amplifier, the CMOS receiver is gain-limited rather than noise-limited [46]. What we mean by gain-limited receiver is that for a given system bandwidth the receiver gain-bandwidth product is limited such that it cannot provide very high gains. However, the voltage level that the receiver circuit needs to output is still quite high so to achieve the required output voltage level, the receiver requires high optical power at its input. This input optical power level is much higher than the noise floor of the receiver so it is the required gain from the receiver that dictates the minimum input optical power rather than the receiver's noise level. Then we can assume that an FSOI with a VCSEL amplifier will have its noise performance limited by the amplifier and not the remaining components.

To find the system BER limited by the VCSEL amplifier, we need to measure the SNR of the amplifier. The method to convert the SNR information to BER can be found in many textbooks, and the derivation given below is a modified version of that given in [47].

For a digital transmission (i.e. binary encoding), let $P_{out}(0)$ and $P_{out}(1)$ be the amplifier's mean output power levels and σ_0 and σ_1 be the rms noise power for the binary '0' and '1', respectively (Figure V.15).

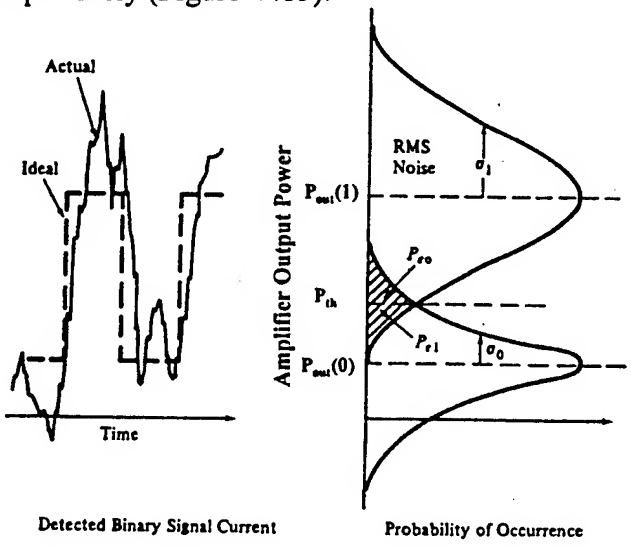


Figure V.15 Error probability for each binary state.

The noise power is normalized to the detector frequency. In other words, the noise power equals the spontaneous emission power in the frequency spectrum that is centered at the signal frequency and extends to either side by as much as the detector frequency (i.e. the bandwidth of the signal transmission). If the frequency of the spontaneous emission is outside this band, then the photocurrent caused by the beating of this noise and the signal will be at a higher frequency than the electronics can respond to, so it will be averaged out to zero.

The shaded areas of P_{e0} and P_{e1} are the error probabilities for each state and are given as (assuming a Gaussian distribution for the noise)

$$P_{e0} = \text{erfc}\left(\frac{P_1 - P_{th}}{\sigma_1}\right) \quad ; \quad P_{e1} = \text{erfc}\left(\frac{P_{th} - P_0}{\sigma_0}\right)$$

Equation V.39

P_{th} is the decision threshold level, and is assumed to be adjusted so that $P_{e0} = P_{e1}$. The error function in Equation V.39 is defined as

$$P_e = \text{erfc}(Q) = \frac{1}{\sqrt{2\pi}} \int_Q^\infty \exp\left(-\frac{Z^2}{2}\right) dZ$$

Equation V.40

Since P_{th} is adjusted to have the error probabilities equal for the two binary states, we have $P_{e0} = P_{e1}$ and $P_e = 1/2(P_{e0} + P_{e1})$ so we get

$$P_e = \text{erfc}\frac{P_1 - P_0}{\sigma_0 + \sigma_1}$$

Equation V.41

The noise in either binary state consists of quantum noise and amplifier noise, and for σ_0, the quantum noise goes to zero. However, we assume that for the '1' state, the amplifier noise dominates the quantum noise so we can let $\sigma_0 \sim \sigma_1$. Then Equation V.41 can be rewritten as a function of the amplifier's SNR measured at the '1' state

$$P_e = \text{erfc}\frac{SNR_{amplifier}}{2}$$

Equation V.42

The BER due to the VCSEL amplifier as a function of the amplifier SNR at the '1' state is plotted in Figure V.16. The BER of 10^{-15} (for data communication systems) and the corresponding required SNR are marked on the graph.

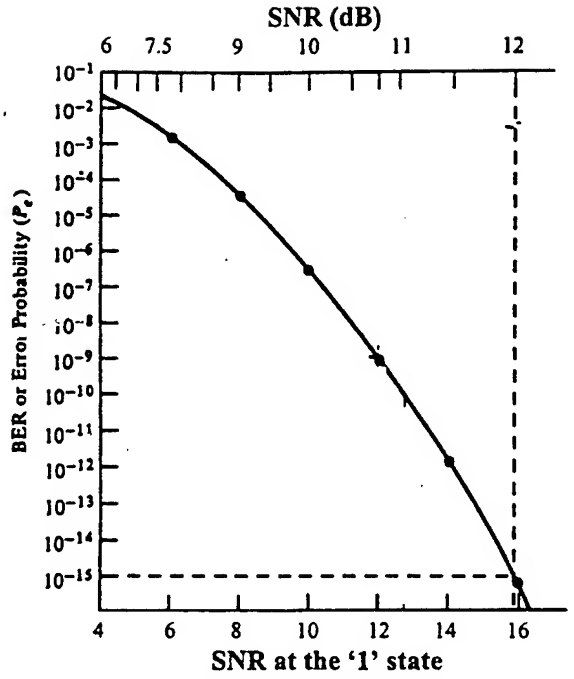


Figure V.16 Conversion of signal-to-noise ratio to bit-error-rate.

As can be seen from Figure V.16, for the most demanding data communication systems, a system BER of 10^{-15} requires that the amplifier have at least 12 dB of SNR at its '1' state. In the next section, we measure the SNR of the VCSEL amplifier and show that even at high bandwidths of 10 GHz, the amplifier noise is sufficiently low to provide such bit-error-rates.

V.5.2. SNR measurement of a VCSEL amplifier

To measure the signal to noise ratio of the VCSEL amplifier, an input beam of 1 μW is coupled into an amplifier. This input power level is slightly lower than what is expected to be used in a practical FSOI system (~2 - 3 μW); therefore, it is ensured that the quoted BER below will hold in future systems.

The VCSEL used for this experiment is single mode at threshold, and it has its maximum gain at its threshold (I_{bias} = 2.54 mA). The amplified output signal is then detected by a multiwavelength meter (Hewlett-Packard Model No. HP 86120B), and its signal to noise ratio is measured to be 11.7 dB for a noise bandwidth of 0.1 nm. In this experiment, the frequency at which the detected optical power is at its peak is measured (i.e. center frequency). Then the two frequencies on either side of the center frequency at which the signal power drops by 10 dB (i.e. to ~ 1 / e^2) below the peak intensity mark the signal spectrum. The total signal power is then defined to be the power that lies inside the signal spectrum. The noise power, on the other hand, is normalized to a bandwidth of 0.1 nm. At λ = 850 nm, this corresponds to a bandwidth of ~40 GHz. However, the application of VCSEL amplifiers are meant to be on the order of GHz, so the relevant noise bandwidth is assumed to be limited to 10 GHz, which effectively increases the SNR by another 6 dB to 17.7 dB. In this case, note that

the amplifier is able to provide the required 12 dB of SNR for a BER of 10^{-15} with ~ 5.7 dB remaining for the receiver noise margin. Furthermore, the typical fiber communication bandwidth at the present is 2.5 GHz, so if such a lower bandwidth was assumed for the free-space system, the noise bandwidth would be reduced by another factor of 4, and the SNR would be increased by another 6 dB.

Although the SNR was high in this experiment, the nominal output power was not stable when the device was biased exactly at its threshold. In other words, even without the input optical beam, the device could go into lasing, and the bit error rate at the detector could be significantly lowered because of these random fluctuations of the VCSEL output. To accommodate for this fluctuation, the amplifier was biased slightly below threshold (I_{bias} = 2.45 mA). In this case, the gain of the amplifier dropped to approximately 85% of its peak value and the SNR of the amplifier dropped by 2 dB to ~15.7 dB, still allowing 3.7 dB of noise degradation for the receiver. In return, the fluctuations of the VCSEL output in the absence of external modulation due to amplified spontaneous emission were eliminated.

V.5.3. Improvement in SNR with a volume hologram and/or polarizer

In some applications, the required BER may be lower or the receiver noise performance may be worse. In these cases, the SNR of the VCSEL amplifier can be further improved by placing a polarizer and/or a volume hologram at the amplifier output (before the detector). This approach is based on the fact that the signal is coherent and linearly polarized whereas the spontaneously emitted photons are incoherent and unpolarized. Since the diffraction efficiency of the volume hologram depends on the coherence length of the input beam, the signal beam can be diffracted very efficiently at a certain angle and a large portion of the spontaneously emitted photons will pass through the hologram untouched. If we place the detector off-axis from the amplifier such that it collects the diffracted signal beam, then a fraction of the spontaneously emitted photons will never be detected and the SNR of the amplifier output can be improved. Similarly, if a polarizer parallel to the signal polarization is inserted or an anisotropic material is used for the hologram, the noise due to spontaneous emission in the orthogonal polarization can be further filtered out.

The volume hologram used in our experiments was recorded on a polymer-based holographic material sensitive to 850 nm [48]. The diffraction efficiency was measured at ~91% so the output signal power does not suffer much, but the SNR of the amplifier is significantly improved. The Ti:Sa laser was used for the recording since the light output power from the VCSEL was not sufficient. However, the sensitivity of the material is being improved and it is predicted that we will be able to record with ~100 μW of light power or less. In this case, the spatial mode structure of the VCSEL at the operating bias current can be in-situ recorded into the hologram such that the filtering of the spontaneous emission will be improved.

The effects of inserting the polarizer and the volume hologram were measured separately and together. The improvement in the SNR of the VCSEL amplifier was measured to be 1.7 dB for the polarizer and 0.8 dB for the volume hologram for a total of 2.5 dB improvement when both were utilized simultaneously. Comparing with the

SNR measurements of the previous section, the allowed noise margin for the receiver was increased from 3.7 dB to 6.2 dB, which is easily feasible with the present CMOS receivers.

V.6. Conclusion

A simple procedure, which is used to model the small-signal behavior of a semiconductor laser as an equivalent electrical circuit, is first applied to an electrically modulated laser, and the resulting equivalent circuit is verified to be exactly the same as that given in the literature. The procedure is then used to model the laser behavior under optical modulation (i.e. when the laser is used as an optical amplifier). Finally, the model is extended to include multi-mode operation of the laser. In all cases, it is shown that the voltage and current equations of the electrical circuits are exactly equivalent to the small-signal rate equations of the semiconductor laser.

The electrical circuits presented in the previous sections are exact models for a multi-mode semiconductor laser under external modulation (electrical and/or optical), as long as the small-signal assumption is not violated (i.e. the modulation range is small compared to the equilibrium values at the given bias condition). Therefore, these circuits provide a fast and accurate simulation tool with very little computational complexity for small-signal laser behavior. These circuits can further be used in combination with more advanced optoelectronic computer-aided-design (CAD) programs, which use mathematical techniques to obtain large-signal behavior of a laser through piecing together small-signal behaviors at various regimes.

In this appendix, an equivalent electrical circuit is used to derive an analytical expression for the maximum gain-bandwidth product of a VCSEL amplifier, which is proportional to the photon loss rate from the output mirror. Optimum biasing conditions and the optimum amplifier structure are examined, and the theory is verified experimentally. A steady-state cavity gain of 23 dB is demonstrated.

From the theory, an optimum structure is proposed. The optimum amplifier consists of a VCSEL biased at its threshold, which operates in a single mode. The mirror reflectivities are lowered up to the point where the optical gain from the quantum wells exactly cancels the loss from the mirrors (i.e. where threshold can barely be reached). For a VCSEL with an optical gain of 5000 cm^{-1} in the active quantum wells, the optimum mirror reflectivities are 96.7% and 98.3% for a maximum gain-bandwidth product of 556 GHz.

Finally, a method is proposed to use the VCSEL amplifier structure as an ultra low voltage (~ 50 mV), high contrast ratio (> 10:1), high speed (> 1 GHz) optical light modulator for future transmitter applications, where lower voltage swings are required both for scaled down CMOS technologies and for superconducting environments.

The signal to noise ratio of the VCSEL amplifier was measured to be 17.7 dB at its threshold (i.e. where gain is maximum) in the presence of a 1 μW external input beam and taking the detector cutoff frequency to be 10 GHz. The SNR could be further increased by 2.5 dB by inserting a polarizer and a volume hologram between the amplifier and the detector to filter out some of the spontaneously emitted photons since these photons are unpolarized and incoherent, whereas the signal is at a given polarization and is coherent. Finally, to eliminate the random fluctuations of the

VCSEL output due to amplified spontaneous emission, the device is biased slightly below threshold, sacrificing approximately 15% of the gain and 2 dB of SNR in return for output power stability.

As a result, the overall SNR was ~ 18.2 dB when biased slightly below threshold (i.e. with stable output power). Compared to the required SNR of 12 dB, the VCSEL amplifier can satisfy a bit error rate of 10^{-15} in data communication systems while allowing a > 6 dB noise margin for the receiver.

Acknowledgement:

Section V.2 of this Appendix, in part, is a reprint of the material as it appears in "Small signal equivalent circuits for a semiconductor laser," by Osman Kibar, Daniel Van Blerkom, Chi Fan, Philippe J. Marchand, and Sadik C. Esener in *Applied Optics*, vol. 37, pp. 6136-6139, Sep. 1998. The dissertation author was the primary investigator and first author of this paper.

Section V.3 of this Appendix, in part, is a reprint of the material "Theory and experiment for the gain-bandwidth product of a VCSEL amplifier," by Osman Kibar and Sadik C. Esener, submitted for publication to Applied Optics (Dec. 1998). The dissertation author was the primary investigator and first author of this paper.

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